WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

400G QSFP-DD SR4.2 Bi-Directional Transceiver
P/N: WST-QD4-SRB-MC

Features:

- 400 Gb/s aggregate data rate
- QSFP-DD form factor with 8 × 53.125 Gb/s PAM4 electrical interface
- Bi-Directional optical interface over multimode fiber
- Transmission distance up to 70 m over OM3, 100 m over OM4, and 150 m over OM5 MMF
- MPO-12/APC optical connector
- Single +3.3 V power supply
- Maximum power consumption 12 W
- Operating case temperature: 0 to 70 °C
- RoHS compliant

Applications:

- 400G Ethernet links
- QSFP-DD SR4.2 point-to-point communication
- QSFP-DD SR4.2 to 4 × QSFP28 SR1.2 breakout communication
- Data center interconnects

Standards:

- QSFP-DD MSA compliant
- IEEE 802.3 400GBASE-SR4.2 optical interface
- Class 1M laser product according to EN 60825-1: 2014 and 21 CFR 1040.10

Description

This product is a 400 Gb/s QSFP-DD Bi-Directional optical transceiver module designed for short-reach multimode fiber transmission. It converts eight host electrical data lanes into bi-directional optical lanes and converts the received optical signals back into eight electrical output lanes.

The module uses an MPO-12/APC optical connector and a 76-pin QSFP-DD MSA-compliant edge connector. It operates from a single +3.3 V power supply and supports digital diagnostic monitoring through a 2-wire serial interface.

Functional Description

This product supports up to 425 Gb/s bit rates in a QSFP-DD Bi-Directional optical module. The optical interface uses two wavelength groups, with 850 nm VCSEL transmitters for one group and 910 nm VCSEL transmitters for the other group. On the receiver side, the module converts optical input signals into eight CML-compatible electrical output lanes. The functional block diagram is shown on page 6.

The module supports QSFP-DD SR4.2 point-to-point communication and QSFP-DD SR4.2 to 4 × QSFP28 SR1.2 breakout communication. It operates from a single +3.3 V power supply, with all power supply pins applied concurrently. As defined by the QSFP-DD MSA, the module provides low-speed control and monitoring pins, including ModSelL, SCL, SDA, ResetL, InitMode, ModPrsL, and IntL. The 2-wire serial interface allows the host to access the module memory map and digital diagnostic information.

Absolute Maximum Ratings

Data Rate Specifications	Symbol	Min	Typ.	Max	Unit	Notes
Storage Temperature	TS	-40		+85	°C	
Supply Voltage	VCCT, R	-0.5		3.6	V	
Relative Humidity (non-condensing)	RH	0		85	%	
Damage Threshold, each Lane	THd			3.4	dBm	1

Note:

1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Case operating Temperature	TC	0		70	°C	
Supply Voltage	VCC	+3.135	3.3	+3.465	V	
Electrical Data Rate, each Lane		26.5625 ± 100 ppm			GBd	PAM4
Optical Data Rate, each Lane		26.5625 ± 100 ppm			GBd	PAM4
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance with OM3	D	0.5		70	m	2, 3
Link Distance with OM4	D	0.5		100	m	2, 3
Link Distance with OM5	D	0.5		150	m	2, 3

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.
3. Connector type is APC

Electrical Characteristics (T_{OP}= 0 to 70 °C, V_{CC} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Consumption				12	W	
Supply Current	Icc			3.63	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	PAM4
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	
Receiver (each Lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	PAM4
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	

Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics (TOP = 0 to 70 °C, V_{CC} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Transmitter						
Signaling rate, each lane		26.5625± 100ppm			GBd	PAM4
Center Wavelength	λ1	844		863	nm	
Center Wavelength	λ2	900		918	nm	
RMS Spectral Width	Δλrms			λ1:0.6 λ2: 0.65	nm	
Average Launch Power, each Lane	PAVG	-6.5		4	dBm	1
Optical Modulation Amplitude (OMA), each Lane	POMA	-4.5		3	dBm	2
Launch power in OMA minus TDECQ, each lane		-5.9			dBm	
Transmitter Dispersion Penalty ,each lane	TDECQ			4.5	dB	3
TDECQ – 10log10(Ceq), each lane				4.5		4
Extinction Ratio	ER	3.0			dB	
RIN12 OMA				-128	dB/Hz	
Optical Return Loss Tolerance	TOL	12			dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Encircled Flux		≥ 86% at 19 μm ≤ 30% at 4.5 μm				5
Receiver						
Signaling rate, each lane		26.5625± 100ppm			GBd	PAM4

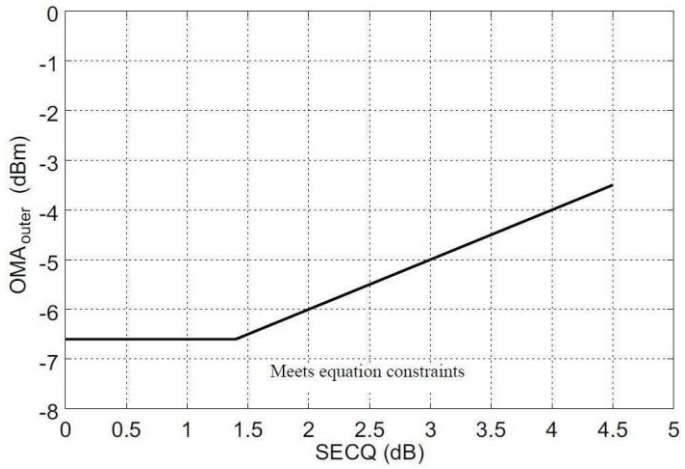
Center Wavelength Lane0	λ1	844		863	nm	
Center Wavelength Lane1	λ2	900		918	nm	
Average Receive Power, each Lane		-8.5		4	dBm	6
Receive Power (OMA), each Lane				3.0	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			Max (-6.6, SECQ – 8)	dBm	8
Receiver Reflectance	RR			-12	dB	
Stressed receiver sensitivity in OMA, each lane				-3.5	dBm	7

Notes:

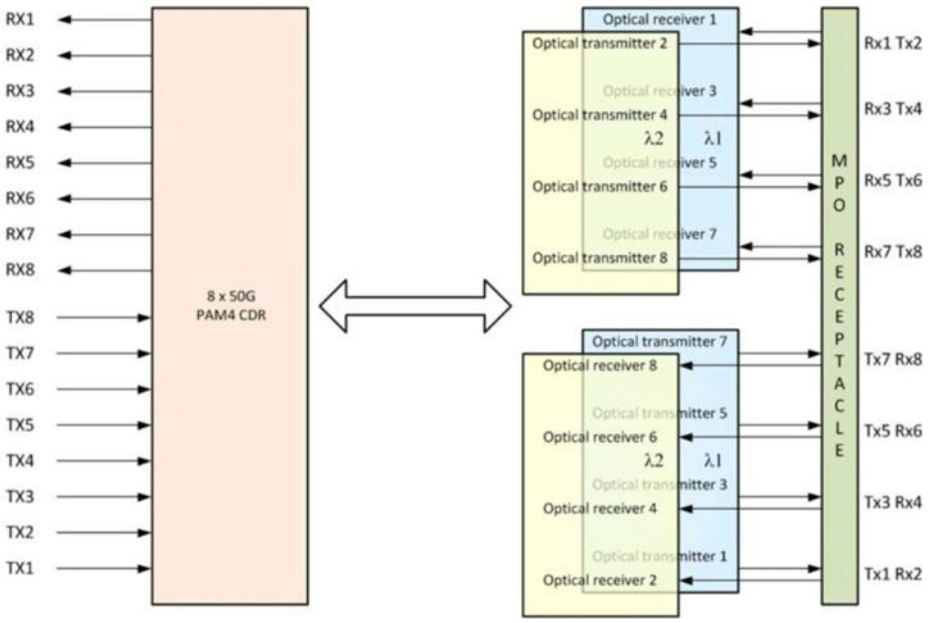
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed this value.
3. TDECq is specified and measured as per IEEE802.3.cm Clause 150.8.5.
4. Ceq is a coefficient defined in IEEE 802.3-2018 Clause 121.8.5.8, which accounts for the reference equalizer noise enhancement.
5. If measured into type A1a.2, or type A1a.3, or type A1a.4, 50 um fibers in accordance with IEC 61280-1-4.
6. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
7. Measured with a conformance test signal at TP3 (see IEEE 802.3 Cl 150) for the BER specified. They are not characteristics of the receiver. The conditions for measuring stressed receiver sensitivity are the following:

Stressed eye closure (SECQ), lane under tes`t	4.5	dB
SECQ – 10log10(Ceq) lane under test (max)	4.5	dBm
OMAouter of each aggressor lane	3.0	dBm

8. These test conditions are for measuring stressed receiver sensitivity. Receiver sensitivity is considered a normative requirement. RX sensitivity is defined for a transmitter with a value of SECQ up to 4.5dB. For transmitter with SECQ different from 4.5dB, limit is reported as per figure 5



Block Diagram



Transceiver Block Diagram

Pin Assignment

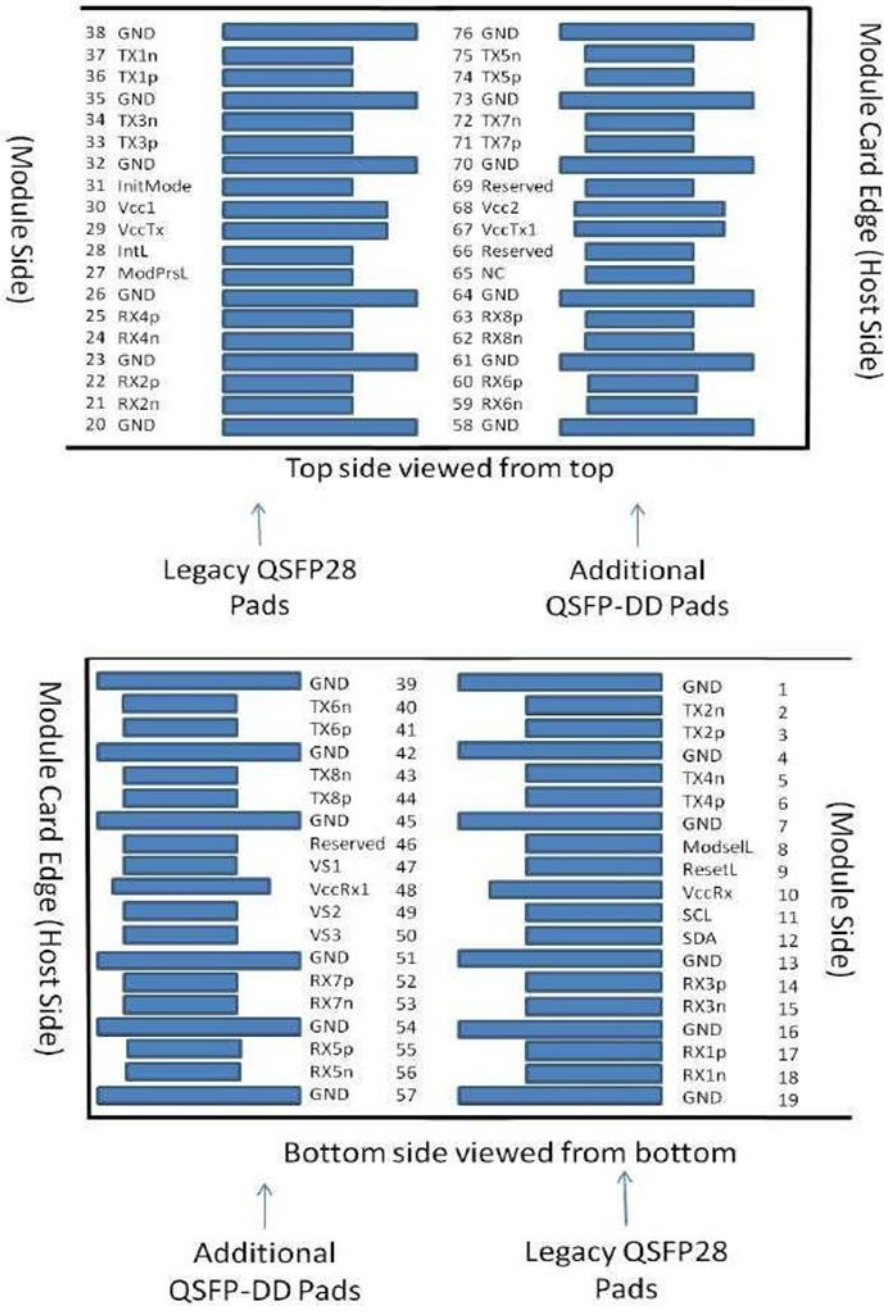


Diagram of Host Board Connector Block Pin Numbers and Name

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B

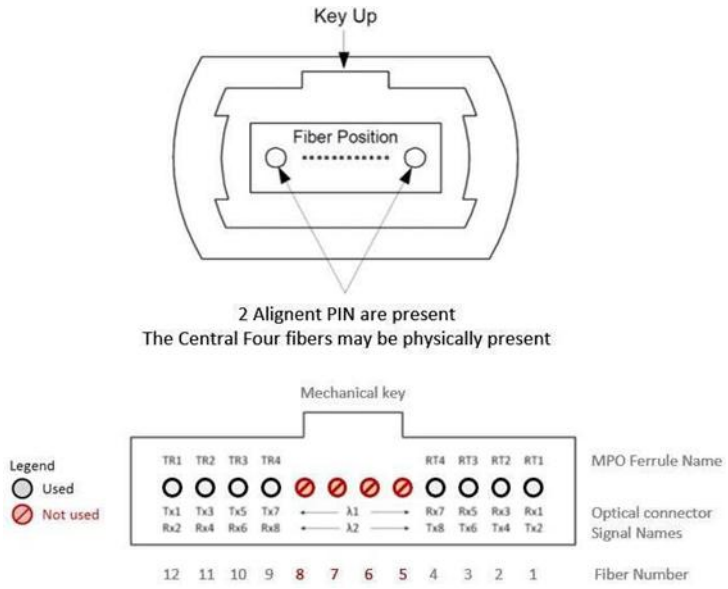
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B

35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A

69		Reserved	For Future Use	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

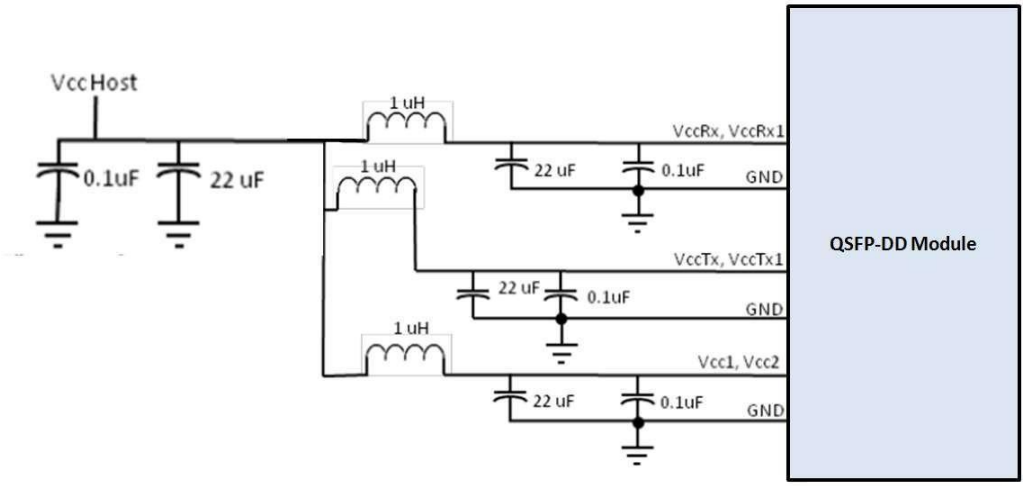
Optical Interface Lanes and Assignment

The following figure shows the orientation of the multi-mode fiber facets of the optical connector. Table 1 provides the lane assignment.

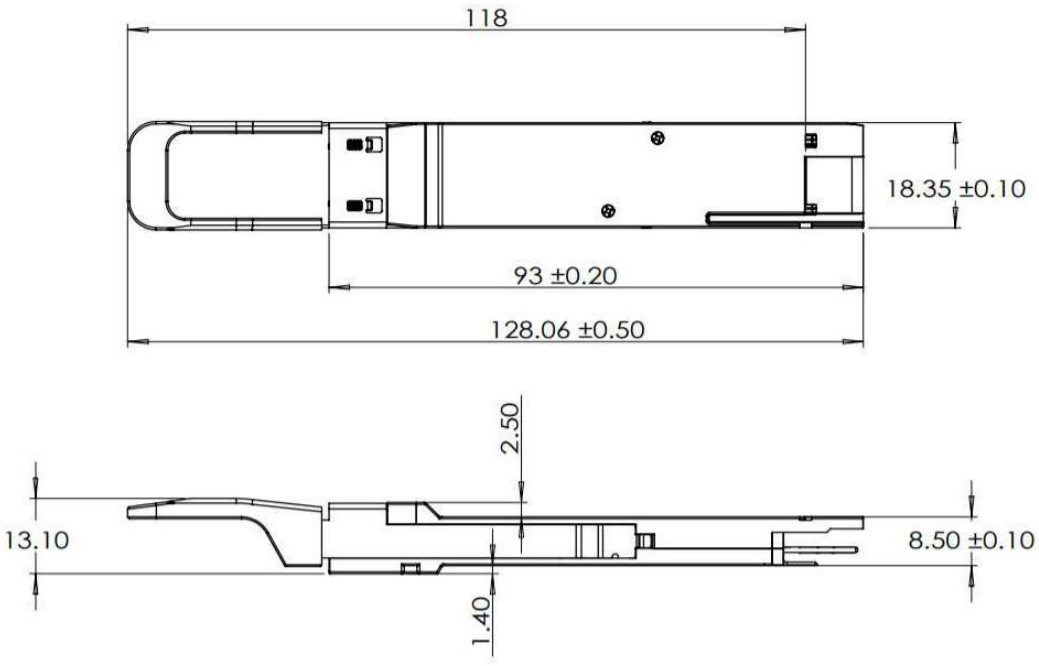


Outside View of the QSFPDD MPO-12 Receptacle

Recommended Circuit



Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification						
	Package	Data rate per Lane	Laser	Reach	Temp.	Application code	Notes
WST-QD4-SRB-MC	QSFP-DD	53.125 Gbps PAM4	850 nm / 910 nm VCSEL	70m OM3 100m OM4 150m OM5 MMF	0 to 70 °C	400GBASE-SR4.2	RoHS DDM

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	17-Jun-2024	New Issue	Ken Cheng	Joanne Ni	Tom Tang
V1.1	08-Oct-2024	Add Connector type APC	Ken Cheng	Joanne Ni	Tom Tang
V1.2	15-Jun-2026	Add OM3/OM4 description Update Photo	Jason Hou	Wayne Liao	Tom Tang

WAVESPLITTER™ TECHNOLOGIES, INC.

Headquarters
16F-5, No. 75, Sec. 1, Xintai 5th Rd., Xizhi Dist.,
New Taipei City 22101, Taiwan
Tel: +886-2-2698-7208
Fax: +886-2-2698-7210
Email: sales@wavesplitter.com
Website: https://wavesplitter.com/