WAVESPLITTER™
TECHNOLOGIES, INC.

Data Sheet

400G QSFP-DD SR8 100 m Transceiver Module
P/N: WST-QD4-SR8-C

Features:

- Hot pluggable QSFP-DD form factor
- 400 Gb/s aggregate data rate
- 8 optical lanes at 53.125 Gb/s PAM4
- 8 electrical lanes at 53.125 Gb/s PAM4
- 8-lane parallel VCSEL transmitters and PIN photodiode receivers with TIAs
- MPO-16/APC optical connector
- SR8 (100 m) optical interface over OM4 multimode fiber with host-side KP4 FEC
- Single 3.3 V power supply
- Power consumption: Max. 8 W
- Operating case temperature: 0 °C to +70 °C
- Digital diagnostic monitoring (DDM) support
- RoHS compliant

Applications:

- 400 Gigabit Ethernet links over multimode fiber
- Data center interconnect applications
- Switch-to-switch and switch-to-router interconnections

Standards:

- IEEE 802.3cd and IEEE 802.3bs compliant
- QSFP-DD MSA compliant
- OIF CEI-56G-VSR-PAM4 compliant
- CMIS 4.0 management interface compliant

Description:

The WST-QD4-SR8-C module is a 400 Gb/s QSFP-DD optical transceiver module designed for short-reach multimode fiber (MMF) transmission. It provides eight electrical lanes operating at 53.125 Gb/s PAM4 signaling and supports an SR8 optical interface for transmission distances up to 100 m over OM4 multimode fiber. The module integrates optical and electrical components within a QSFP-DD form factor and uses an MPO-16/APC connector for optical connectivity. The transmitters are based on 850 nm VCSEL lasers and the receivers use PIN photodiodes with TIAs, optimized for short-reach multimode fiber applications.

The module converts 8 × 53.125 Gb/s PAM4 electrical input signals into 8 optical output lanes, enabling 400 Gigabit Ethernet links over multimode fiber. It is designed for operation with host-side KP4 forward error correction (FEC) to meet link performance requirements. The module supports digital diagnostic monitoring (DDM) through the QSFP-DD management interface, enabling real-time monitoring of key operating parameters.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum Supply Voltage	V_{cc}	-0.5		3.6	V	
Storage Temperature	T_{sto}	-40		85	°C	
Relative Humidity	RH	5		85	%	Non-condensing

Operating Environment

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Electrical Signal Rate, each lane		26.5625 ± 100 ppm			GBd	
Optical Signal Rate, each lane		26.5625 ± 100 ppm			GBd	
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Operating Case Temp.	Tc	0		70	°C	
Power Consumption	Pc			8	W	
Link Distance with OM3	Dl	0.5		70	m	
Link Distance with OM4	D2	0.5		100	m	

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
High Speed Electrical Input Characteristics						
Signaling rate per lane (range)	TP1	-100 ppm	26.5625	+100 ppm	GBd	1
Differential peak-peak input voltage tolerance	TP1a	900			mV	
Single-ended voltage tolerance	TP1a	-0.4		3.3	V	
DC common mode voltage	TP1	-350		2850	mV	2
High Speed Electrical Output Characteristics						
Signaling rate per lane (range)	TP4	-100 ppm	26.5625	+100 ppm	GBd	
AC common-mode output voltage (RMS)	TP4			17.5	mV	
Differential peak-to-peak output voltage	TP4			900	mV	

Near-end ESMW (Eye symmetry mask width)	TP4	0.265			UI	
Near-end Eye height, differential	TP4	70			mV	
Far-end ESMW (Eye symmetry mask width)	TP4	0.2			UI	
Far-end Eye height, differential	TP4	30			mV	
DC common mode voltage	TP4	-350		2850	mV	2

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Transmitter						
Signaling rate per lane (range)		-100 ppm	26.5625	+100 ppm	GBd	
Modulation format			PAM4			
Center wavelength (range)	λ	840	-	860	nm	
RMS spectral width				0.6	nm	1
Average launch power, each lane	P	-6.5		4	dBm	
OMAouter, each lane	P_{OMA}	-4.5		3	dBm	2
Launch power in OMAouter minus TDECQ		-5.9			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				4.5	dB	
Average launch power of OFF transmitter, each lane	Poff			-30	dB	
Extinction ratio, each lane	ER	3			dB	
RIN21OMA	RIN			-128	dB/Hz	
Optical return loss tolerance				12	dB	
Receiver						
Signaling rate, each lane (range)		-100 ppm	26.5625	+100 ppm	GBd	

Modulation format		PAM4				
Center wavelength (range)	λ	840	-	860	nm	
Damage Threshold		5			dBm	3
Average receive power, each lane		-8.4		4	dBm	4
Receive power, each lane (OMAouter)	R_{OMA}			3	dBm	
Receiver reflectance				-12	dB	
Receiver sensitivity (OMAouter), each lane	SEN	max(-6.5, SECQ-7.9)			dBm	
LOS Assert		-30		-13	dBm	
LOS De-Assert				-11	dBm	
LOS Hysteresis		0.5			dB	

Notes:

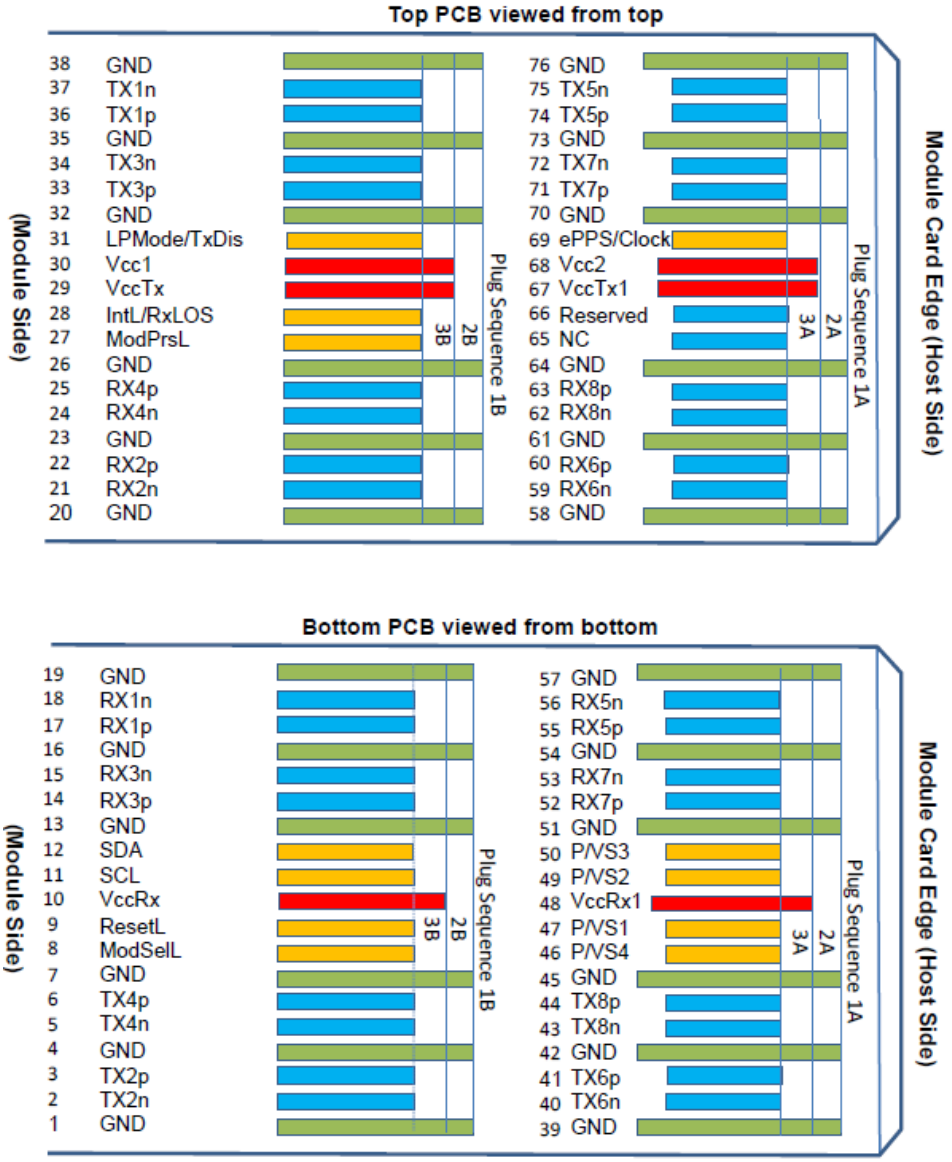
1. RMS spectral width is the standard deviation of the spectrum.
2. If the TDECQ <1.4 dB, the OMA (min) has to exceed this value.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance .

Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions

Parameter	Accuracy	Unit
Measured transceiver temperature	±3	°C
Measured transceiver supply voltage	±3	%
Measured Tx bias current	±10	%
Measured Tx output power	±3	dB
Measured Rx received average optical power	±3	dB

Pin Assignment



Pin out of Connector Block on Host Board

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VCC Rx	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VCC Tx	+3.3 V Power Supply Transmitter	2B	2
30		VCC1	+3.3 V Power Supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	

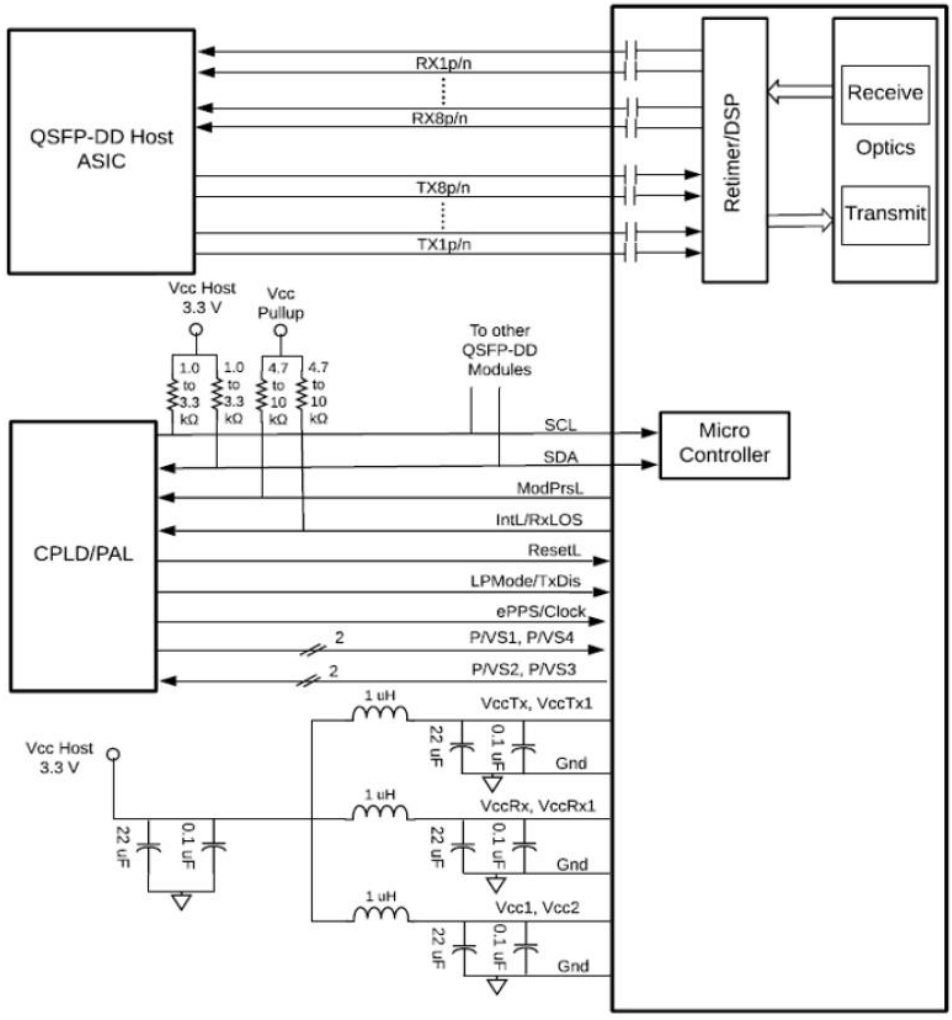
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1B	1

65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VCC Tx1	+3.3 V Power Supply Transmitter	2A	2
68		VCC2	+3.3 V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input (N/C within module)	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

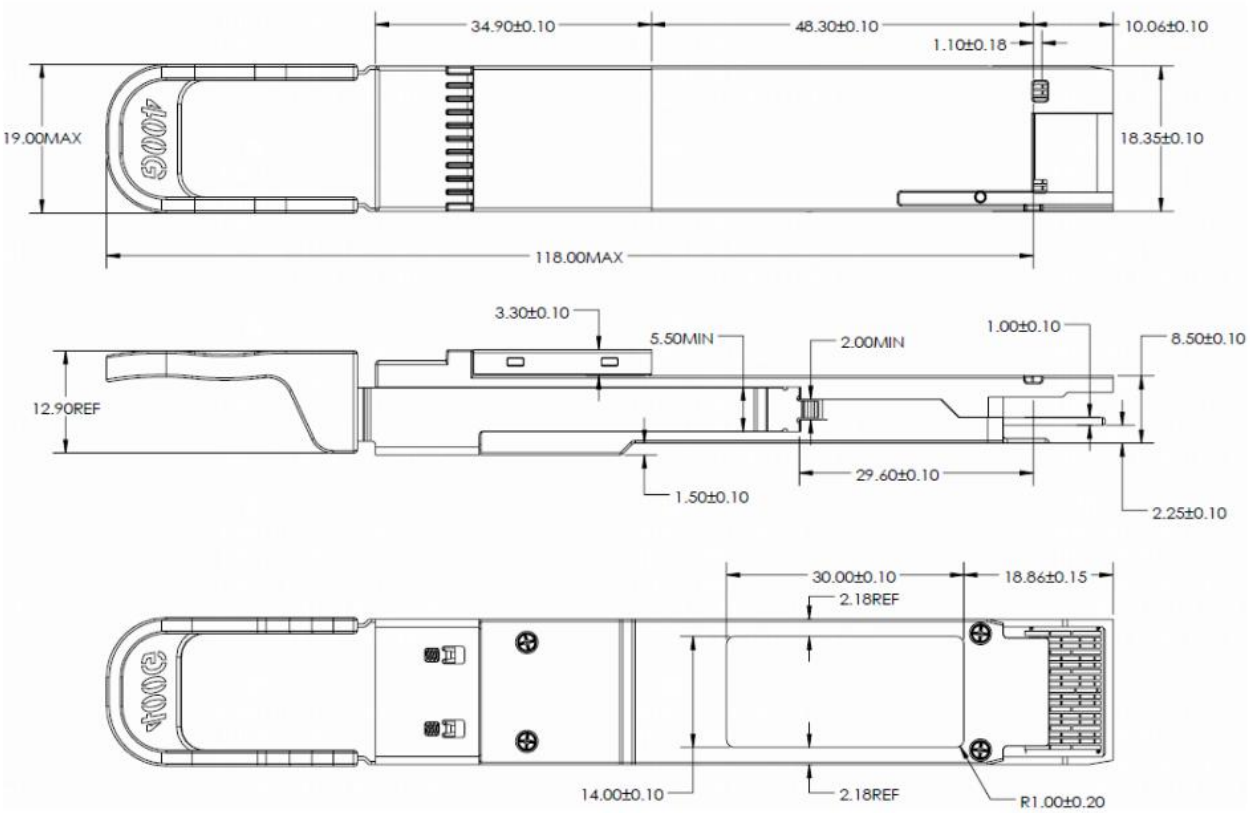
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed above. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Recommended Block Diagram with host board's connections



Mechanical Drawing



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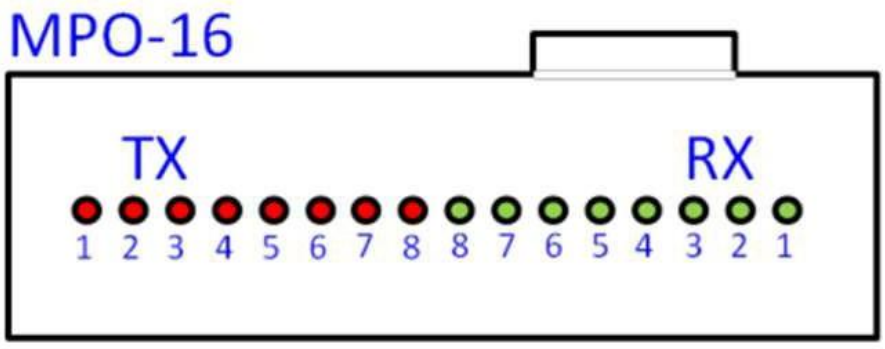

Ordering Information

Part No	Package	Data rate	Reach	Operating Temperature	Application Code	Note
WST-QD4-SR8-C	**QSFP-DD**	**53.125 Gb/s (PAM4) per optical lane**	**100 m**	**0 °C to 70 °C**	**400G Ethernet**	**DDM RoHS**

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	15-Jun-2024	New Issue	Jason Hou	Wayne Liao	Tom Tang

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