Data Sheet

400G QSFP-DD LR4 10km Transceiver Module
P/N: WST-QD4-LR4-C

Features:

- 4 × 106.25 Gb/s PAM4 optical lanes (CWDM)
- 8 × 53.125 Gb/s PAM4 electrical lanes (400GAUI-8)
- Integrated DSP-based signal processing architecture
- Four-channel CWDM EML laser transmitters and PIN photodiode receivers with TIAs
- Duplex LC optical connector
- Up to 10 km transmission over single-mode fiber with host-side FEC
- Single 3.3 V power supply
- Power consumption: 8.5 W (Typ.), 10 W (Max.)
- Operating case temperature: 0 °C to +70 °C
- RoHS compliant

Applications:

- 400 Gigabit Ethernet links over single-mode fiber
- Data center interconnect applications
- Switch-to-switch and switch-to-router interconnections

Standards:

- IEEE 802.3cu and IEEE 802.3bs compliant
- QSFP-DD MSA compliant
- CMIS management interface compliant with CMIS 5.0

Description

The WST-QD4-LR4-C is a hot-pluggable 400G QSFP-DD LR4 optical transceiver designed for 400 Gigabit Ethernet applications over single-mode fiber.

The module supports an eight-lane 53.125 Gb/s PAM4 electrical host interface and four optical lanes operating at 106.25 Gb/s PAM4. A DSP-based signal processing architecture is used to enable signal conversion between the electrical and optical interfaces.

On the transmit side, electrical signals drive four CWDM EML transmitters operating at nominal wavelengths of 1271 nm, 1291 nm, 1311 nm, and 1331 nm. On the receive side, the optical signals are detected by a PIN photodiode array. The optical interface uses a duplex LC connector.

The module supports transmission distances up to 10 km over G.652 single-modefiber and is intended for operation in systems with host-side forward error correction (FEC). It operates from a single 3.3 V power supply and complies with IEEE 802.3cu, IEEE 802.3bs, and QSFP-DD MSA requirements.

Functional Description

The WST-QD4-LR4-C provides electrical-to-optical and optical-to-electrical signal conversion for 400G Ethernet systems based on a QSFP-DD form factor.

The module maps an eight-lane PAM4 electrical host interface to four PAM4 optical lanes and supports operation in systems with host-side forward error correction (FEC), enabling reliable data transmission over single-mode fiber links.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	TS	-40	85	°C	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity	RH	5	85	%	Non-condensation
Receiver Damage Threshold (per lane)	R_D		+6.1	dBm	1

Note1: This parameter defines the maximum optical input power the receiver can withstand without damage and is not an operating condition.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Electrical Signal Rate (per lane)			26.5625		GBd	PAM4 (400GAUI-8)
Optical Signal Rate (per lane)			106.25		Gb/s	
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Operating Case Temperature	T_C	0		70	°C	
Power Consumption	P_C		8.5	10	W	
Link Distance (G.652)				10	km	

Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Test Point	Min	Typ	Max	Unit	Note
High Speed Electrical Input Characteristics						
Signaling rate per lane	TP1	26.5625±100 ppm			GBd	
Differential pk-pk input voltage tolerance	TP1a	900			mV	1
Single-ended voltage tolerance	TP1a	-0.4		3.3	V	
DC common mode voltage	TP1	-350		2850	mV	2

High Speed Electrical Output Characteristics						
Signaling rate per lane	TP4	26.5625±100 ppm			GBd	
AC common-mode output voltage (RMS)	TP4			17.5	mV	
Differential peak-to-peak output voltage	TP4			900	mV	
Near-end ESMW (Eye symmetry mask width)	TP4	0.265			UI	
Near-end Eye height, differential	TP4	70			mV	
Far-end ESMW (Eye symmetry mask width)	TP4	0.2			UI	
Far-end Eye height, differential	TP4	30			mV	
DC common mode voltage	TP4	-350		2850	mV	2

Notes:

1. With the exception to IEEE802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.
3. Other electrical characteristics refer to the latest protocol requirements of 802.3bs Annex 120E

Optical Characteristics (Under Recommended Operating Conditions)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Signaling rate, each lane (range)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths (range)	λ0	1264.5	1271	1277.5	nm	
	λ1	1284.5	1291	1297.5	nm	
	λ2	1304.5	1311	1317.5	nm	
	λ3	1324.5	1331	1337.5	nm	
Total average launch power	P_{OUT}			11.1	dBm	
Average launch power, each lane	P	-2.7		5.1	dBm	1
OMAouter each lane	P_{OMA}				dBm	
for TDECQ <1.4 dB		0.3		4.4		
for 1.4 dB ≤ TDECQ ≤ 3.4 dB		-1.1+TDECQ		4.4		

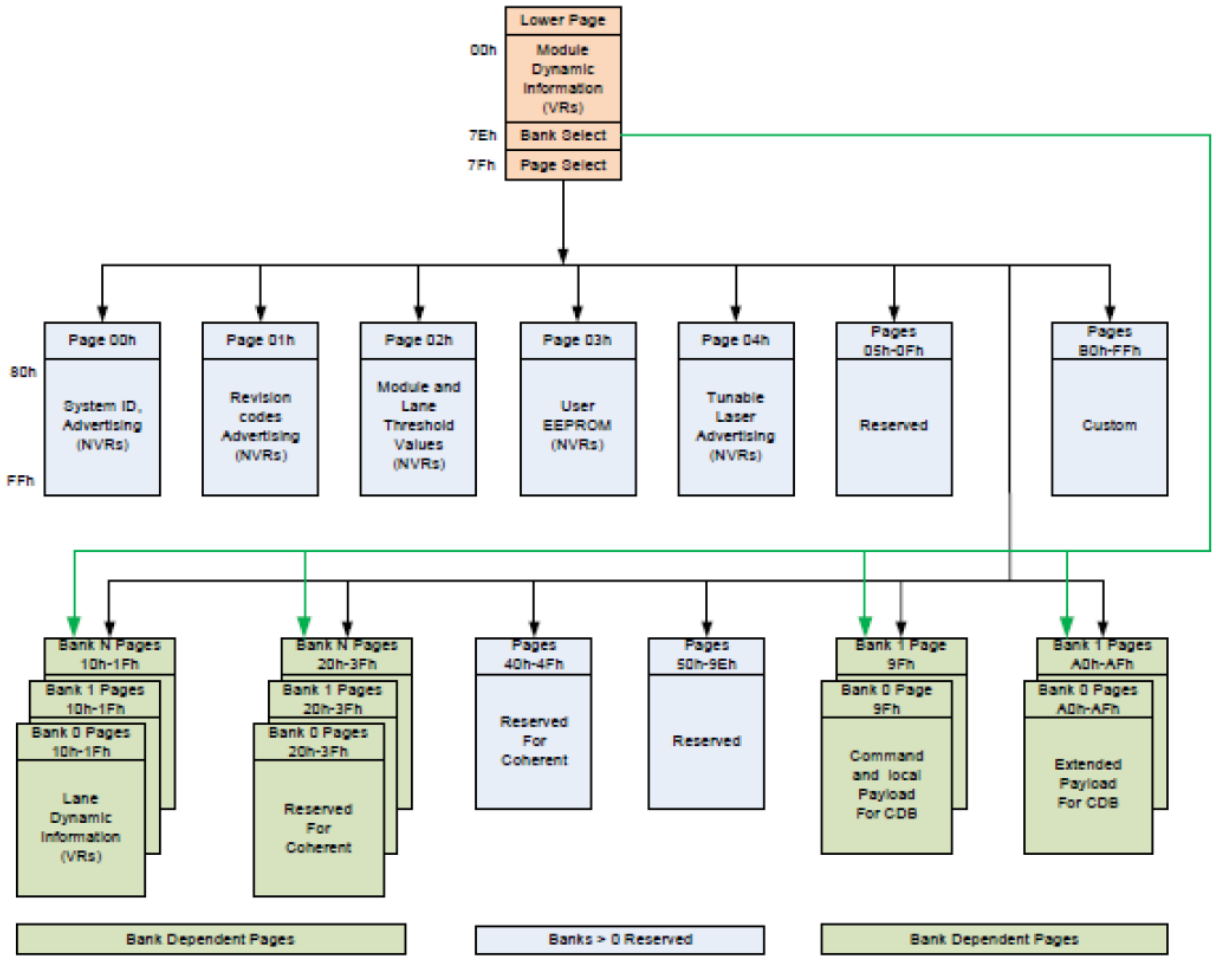
Difference in launch power between any two lanes (OMAouter)				4	dB	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				3.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane				3.4	dB	
| TDECQ – TECQ |				2.5	dB	
Over/under-shoot				22	%	
Transmitter power excursion				2.5	dBm	
Side-mode suppression ratio (SMSR)		30			dB	
Extinction ratio	ER	3.5			dB	
Transmitter transition time				17	ps	
Average launch power of OFF transmitter, each lane	P_{off}			-16	dBm	
$RIN_{15.6}OMA$ (max)	RIN			-136	dB/Hz	
Optical return loss tolerance				15.6	dB	
Transmitter reflectance				-26	dB	2
Receiver						
Signaling rate, each lane (range)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths (range)	λ0	1264.5	1271	1277.5	nm	
	λ1	1284.5	1291	1297.5	nm	
	λ2	1304.5	1311	1317.5	nm	
	λ3	1324.5	1331	1337.5	nm	
Average receive power, each lane		-9		5.1	dBm	3
Receive power, each lane (OMAouter)	ROMA			4.4	dBm	
Difference in receive power between any two lanes, (OMAouter)				4.3	dB	
Receiver Reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane	SEN	max(-6.8, TECQ-8.2)			dBm	
Stressed receiver sensitivity (OMAouter), each lane	SENs			-4.8		4

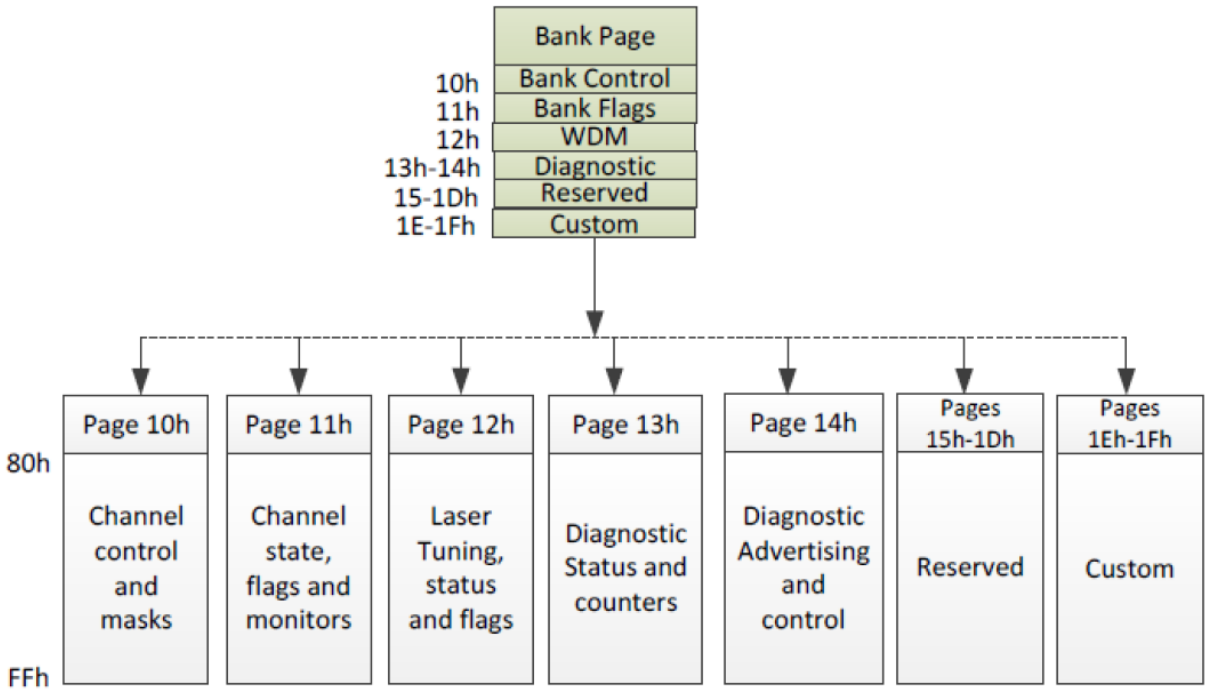
Conditions of stressed receiver sensitivity test:						5
Stressed eye closure for PAM4 (SECQ), lane under test		3.4			dB	
OMAouter of each aggressor lane		-0.4			dBm	
LOS Assert		-26			dBm	
LOS De-Assert				-8	dBm	
LOS Hysteresis		0.5			dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter.
3. Average receive power, each lane(min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. Measured with conformance test signal at TP3 (IEEE 802.3cu 151.8.13) for the BER specified in IEEE 802.3cu 151.1.1 .
5. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

MEMORY MAP (compliant with CMIS Rev. 5.0)

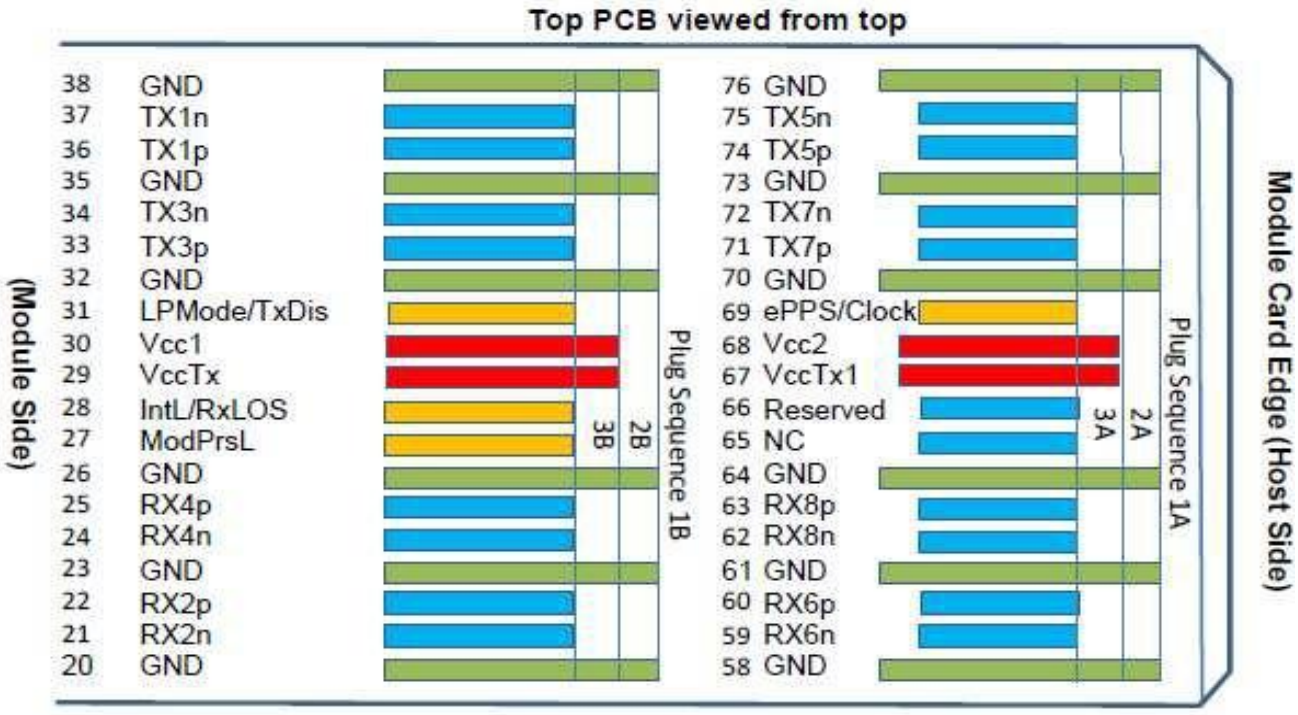


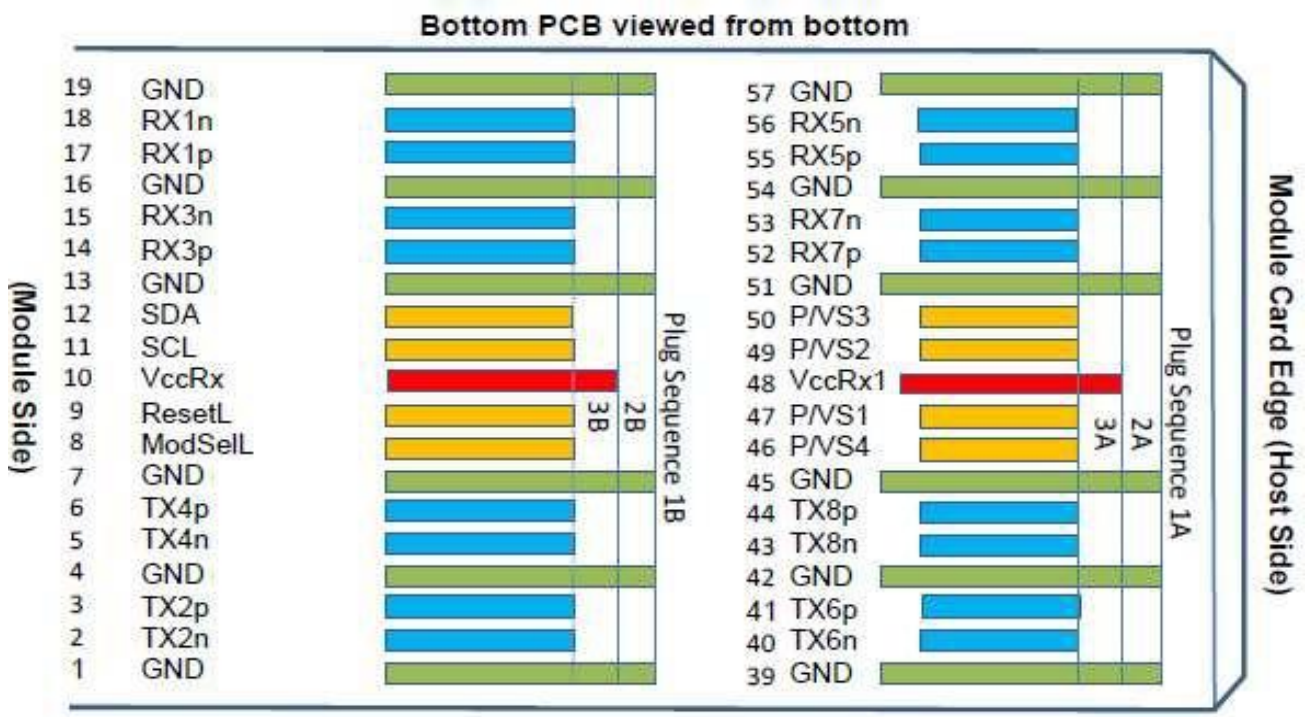


***Digital Diagnostic Monitoring Functions** (Under Recommended Operating Conditions)*

Parameter	Accuracy	Unit	Note
Measured transceiver case temperature	±3	°C	
Measured transceiver supply voltage	±3	%	
Measured Tx bias current	±10	%	
Measured Tx output power	±3	dB	
Measured Rx received average optical power	±3	dB	

Pin Assignment





Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3 V Power Supply Transmitter	2B	2

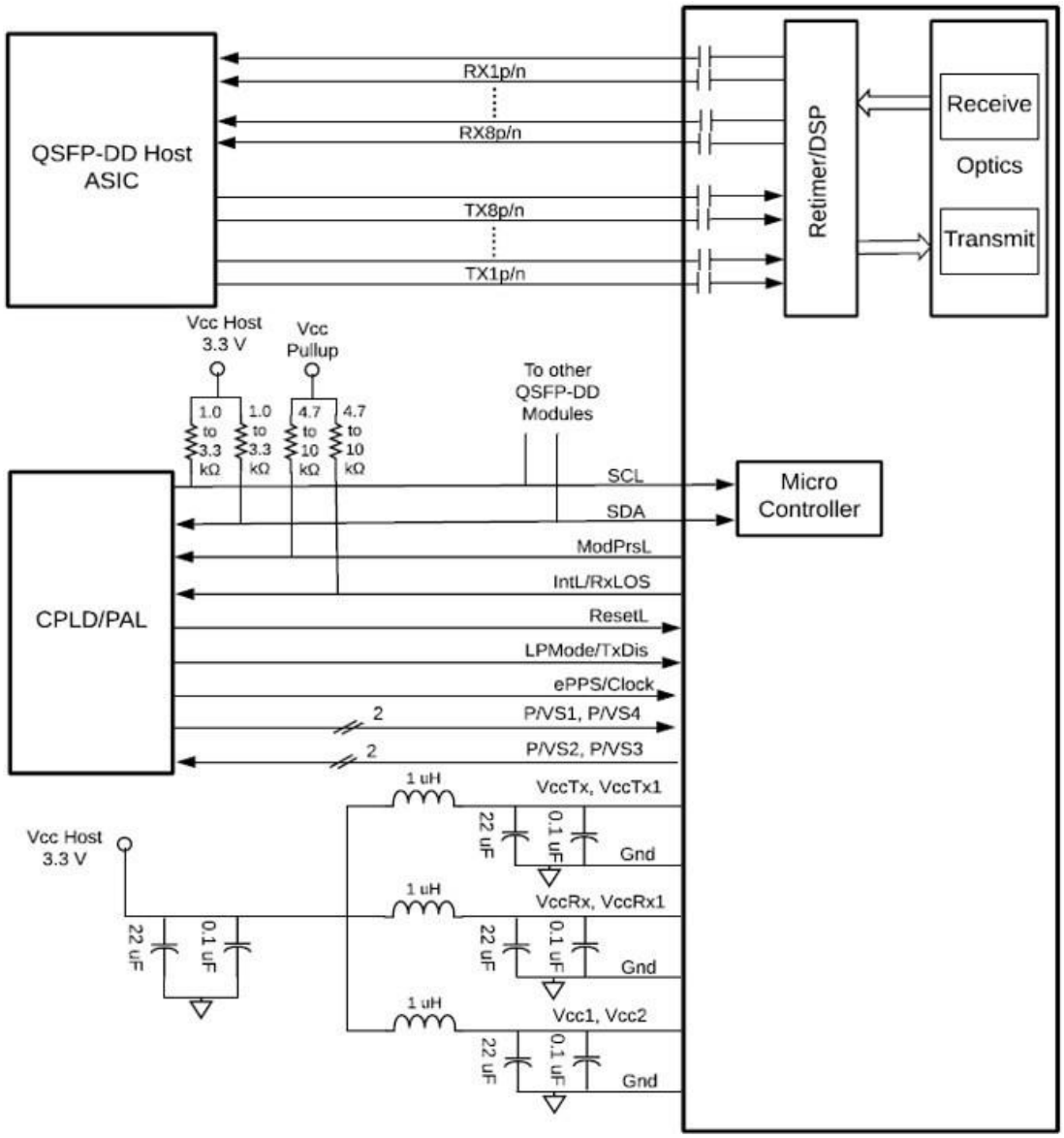
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1

59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1B	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	+3.3 V Power Supply Transmitter	2A	2
68		Vcc2	+3.3 V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference		
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

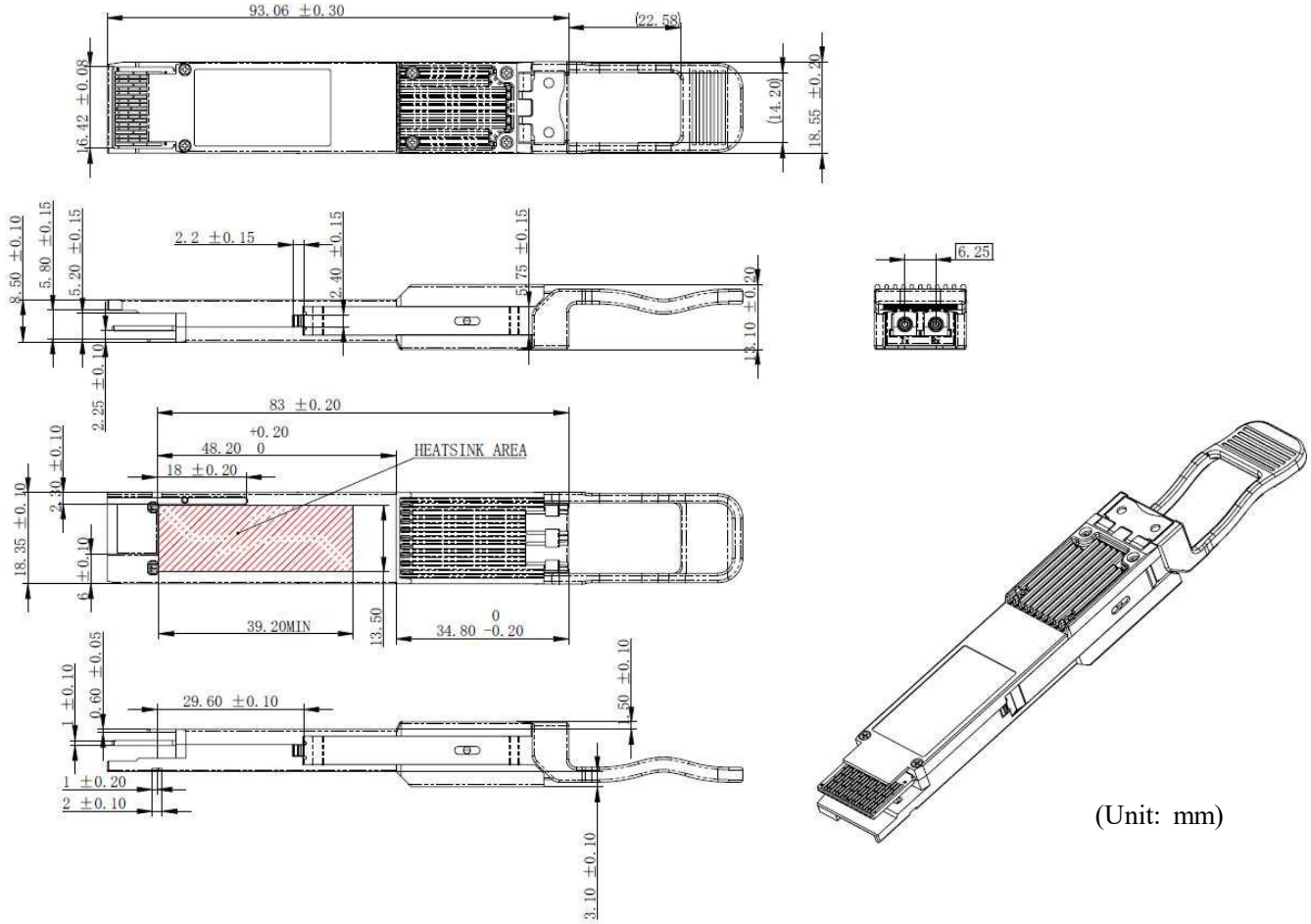
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Pin definitions follow QSFP-DD MSA specifications. Certain signal pins appear in multiple positions to support backward compatibility with QSFP+ and QSFP28 host connectors.

Recommended block diagram with host board's connections



Package Dimensions



(Unit: mm)

Ordering Information

Part No	Package	Data rate	Reach	Operating Temperature	Application Code	Note
WST-QD4-LR4-C	QSFP-DD	106.25 Gb/s (PAM4) per channel	10 km	0 °C to 70 °C	400G Ethernet	DDM RoHS

Modification History

Revision	Date	Description	Originator	Review	Approve
V1.0	20-May-2024	New Issue	Joanne Ni	Wayne Liao	Tom Tang
V1.1	1-Sep-2025	Update CMIS to 5.0	Joanne Ni	Wayne Liao	Tom Tang
V1.2	27-Jan-2026	Revise Power Consumption	Amy Lee	Wayne Liao	Tom Tang

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