

400G QSFP-DD Direct Attach Cable

WS-QD4-DACP_x-xx



Features:

- Up to 26.5625 GBd PAM4 data rate per lane
- 3.3V supply for EEPROM and management interface
- I2C management interface and EEPROM communication
- Hot-pluggable and pull-to-release latch design
- Excellent EMI/EMC performance with 360 degree cable shield termination
- 30 ~ 28 AWG high performance twinax cable
- Low loss, stronger mechanical features, more flexible
- Operating case temperature: -40 to +85 °C
- RoHS Compliant

Applications:

- Data Center & Networking Equipment
- Servers / Storage Devices
- High Performance Computing (HPC)
- Switches / Routers

Standard:

- Compliant with IEEE 802.3cd 400GAUI-8
- QSFP-DD MSA Mechanical and Pinout
- CMIS Management Interface

Absolute Maximum Ratings

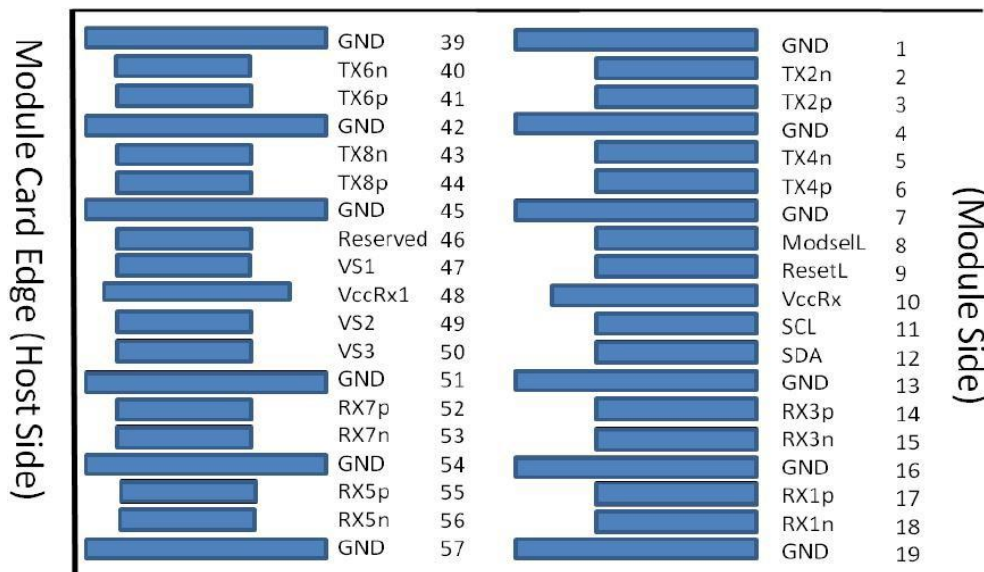
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	T _s	-40		85	°C	
Relative Humidity	RH	5		85	%	Non-condensing
Power Supply Voltage	V _{cc}	0		3.6	V	

Recommended Operating Conditions

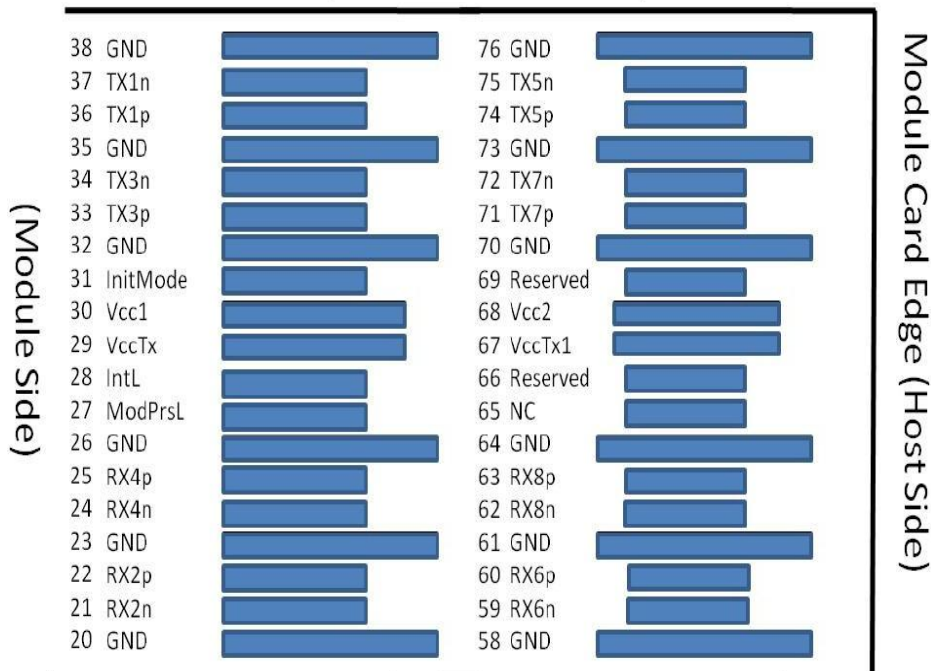
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	T _{case}	-40		85	°C	
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Data Rate	BR		26.5625		GBd	Per lane

QSFP-DD Module Pad Assignments

Bottom side viewed from bottom



Top side viewed from top



Pin	Logic	Symbol	Description	Notes
1		GND	Ground	
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	
12	LVC MOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	

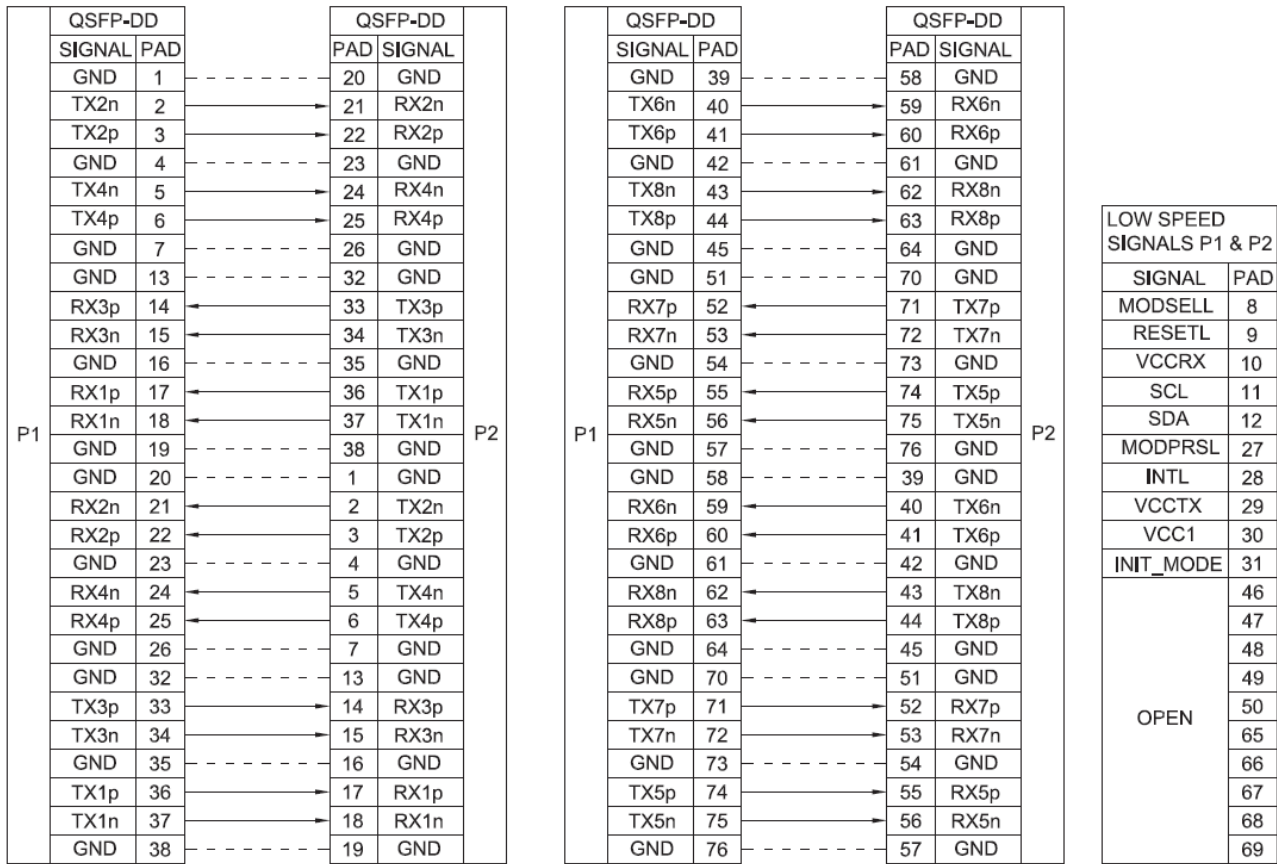
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2

69		Reserved	For Future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

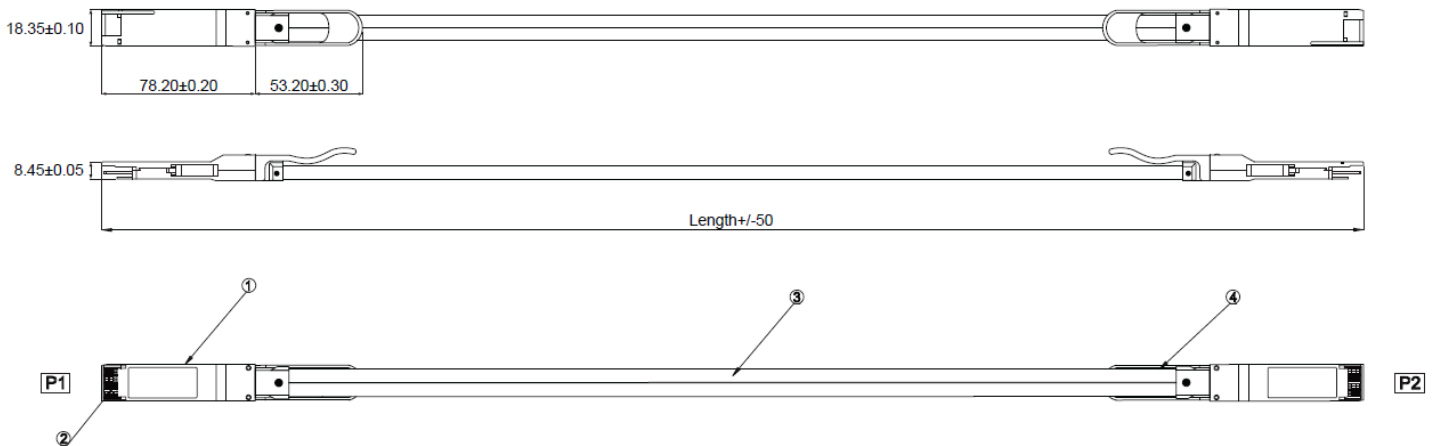
Note:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhm and less than 100 pF.

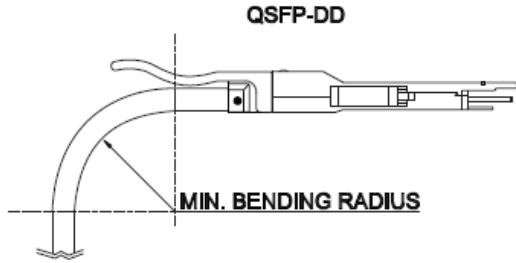
Wiring Diagram



Mechanical Design Diagram



Bending Radius:



Min. bending radius allowed	Repeated	Single
	10 x ϕ	5 x ϕ

Ordering Information

Part No	Specification				
	Package	Data rate per Lane	Temp.	Gauge	Length
WS-QD4-DACP0-0H	QSFP-DD to QSFP-DD	26.5625 GBd PAM4	-40 ~ 85 °C	30 AWG	0.5 m ± 0.05 m
WS-QD4-DACP0-1	QSFP-DD to QSFP-DD	26.5625 GBd PAM4	-40 ~ 85 °C	30 AWG	1.0 m ± 0.05 m
WS-QD4-DACP8-1H	QSFP-DD to QSFP-DD	26.5625 GBd PAM4	-40 ~ 85 °C	28 AWG	1.5 m ± 0.05 m
WS-QD4-DACP8-2	QSFP-DD to QSFP-DD	26.5625 GBd PAM4	-40 ~ 85 °C	28 AWG	2.0 m ± 0.08 m
WS-QD4-DACP8-2H	QSFP-DD to QSFP-DD	26.5625 GBd PAM4	-40 ~ 85 °C	28 AWG	2.5 m ± 0.08 m
WS-QD4-DACP8-3	QSFP-DD to QSFP-DD	26.5625 GBd PAM4	-40 ~ 85 °C	28 AWG	3.0 m ± 0.08 m

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	21-Jun-2019	New Issue	Ivy Chen	Wayne Liao	Wayne Liao
V1.1	01-Jun-2022	Update Drawing	Shao Yu Lee	Tom Tang	Wayne Liao
V2.0	28-Dec-2023	Update drawing, format, and temperature	Ken Chang	Tom Tang	Wayne Liao



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