WAVESPLITTER™
TECHNOLOGIES, INC.

Data Sheet

400G QSFP-DD 1x4 QSFP28 Breakout AOC SMF
P/N: WS-D44Q-AOCxCxx9

Applications:

- 400G to 4×100G Ethernet breakout for data center switching, routers, and AI/HPC clusters
- Short- to medium-reach SMF interconnects inside data centers

Standard:

- IEEE 802.3bs compliant 400GAUI-8 (8×50G PAM4, retimed) and 400GBASE-DR4 optical interface
- IEEE 802.3 compliant 100GBASE-DR optical interface on each QSFP28 end
- QSFP28 host interface: CAUI-4 / 100GAUI-4 (4×25.78125 Gb/s NRZ)
- QSFP-DD MSA & QSFP28 SFF form factor
- CMIS 4.0 management
- RoHS compliant

Features:

- Full-duplex SMF AOC: 1×QSFP-DD to 4×QSFP28
- QSFP-DD electrical: 400GAUI-8, 8×50G PAM4 (retimed)
- QSFP28 electrical (per end): CAUI-4 / 100GAUI-4, 4×25.78125G NRZ
- Optical: QSFP-DD 400GBASE-DR4 (4×53.125 GBd PAM4); QSFP28 100GBASE-DR (1×53.125 GBd PAM4)
- Optical engine implementation
  QSFP-DD DR4 side: integrated SiPh PIC; Tx uses single cooled 1311nm CW DFB laser source with driver mounted to PIC; Rx uses PIN-PD + TIA integrated in PIC
  QSFP28 DR side: Tx single-channel 1310 nm EML; Rx single-channel PIN-TIA
- Connectors: unlocked MPO-12 and 4× Duplex LC
- Supply Voltage +3.3 V
- Cable length: 0.5–50 m
- Operating case temperature: 0°C to +70°C;

Note: Laser/PD implementation may vary by option while maintaining compliance to the specified IEEE optical interfaces.

Descriptions:

The 400G QSFP-DD DR4 to 4×100G QSFP28 DR Active Optical Cable (AOC) is a compact, low-power breakout solution that connects one 400G switch port to four independent 100G ports over single-mode fiber. The QSFP-DD end supports a retimed 8×50G PAM4 400GAUI-8 electrical interface and 400GBASE-DR4 PAM4 optics (4×53.125 GBd, 1310-nm class). Each QSFP28 end provides a dense 100GBASE-DR PAM4 optical engine (1310-nm EA-DFB transmitter, PIN-PD receiver with integrated CDR) with a 4×25.78125 Gb/s NRZ CAUI-4/100GAUI-4 host electrical interface. Integrated DSP/gearbox performs lane aggregation/retiming and supports CMIS 4.0 management.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes.
Maximum Supply Voltage	V_{cc}	-0.5		3.6	V	
Storage Temperature	T_{sto}	-10		70	℃	
Case Operating Temperature	T_{op}	0		70	℃	
Relative Humidity	RH	5		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes.
Operating Case Temperature	TC	0		+70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Dissipation per QSFPDD	Pd			10	W	1
Power Dissipation per QSFP28	Pd			4	W	1
Bit Rate	BR		26.5625		GBaud	2

Note:
1 Per terminal
2 Per channel, PAM4

QSFP-DD Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes
Power Consumption				10	W	
Supply Current	Icc			3.2	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a			900	mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3

Receiver (each Lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

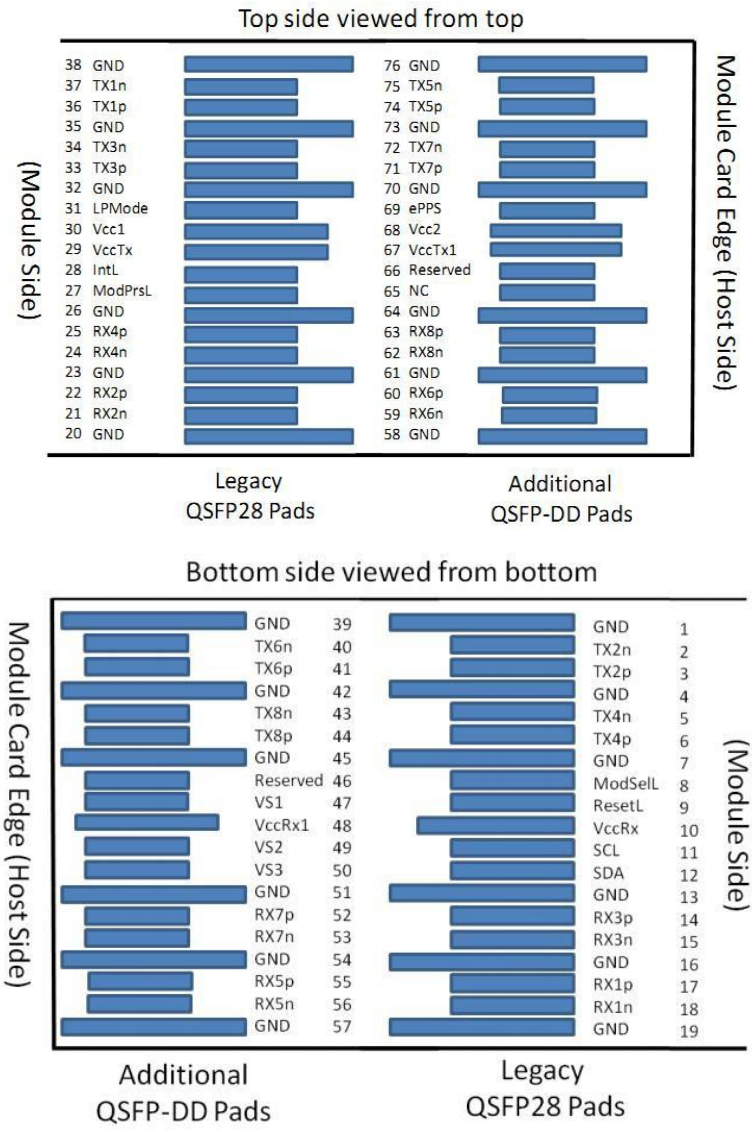
1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage

QSFP28 Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes
Transmitter						
Differential pk-pk input Voltage tolerance				900	mV	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode Voltage		-350		2850	mV	
Receiver						
AC common-mode output Voltage (RMS)				17.5	mV	
Differential output Voltage				900	mV	

Eye width		0.57			UI	
Eye height differential		228			mV	
Vertical eye closure				5.5	dB	
Differential Termination Mismatch				10	%	
Transition Time (min, 20% to 80%)		12			ps	
DC common mode Voltage		-350		2850	mV	

Pin Assignment of QSFP-DD

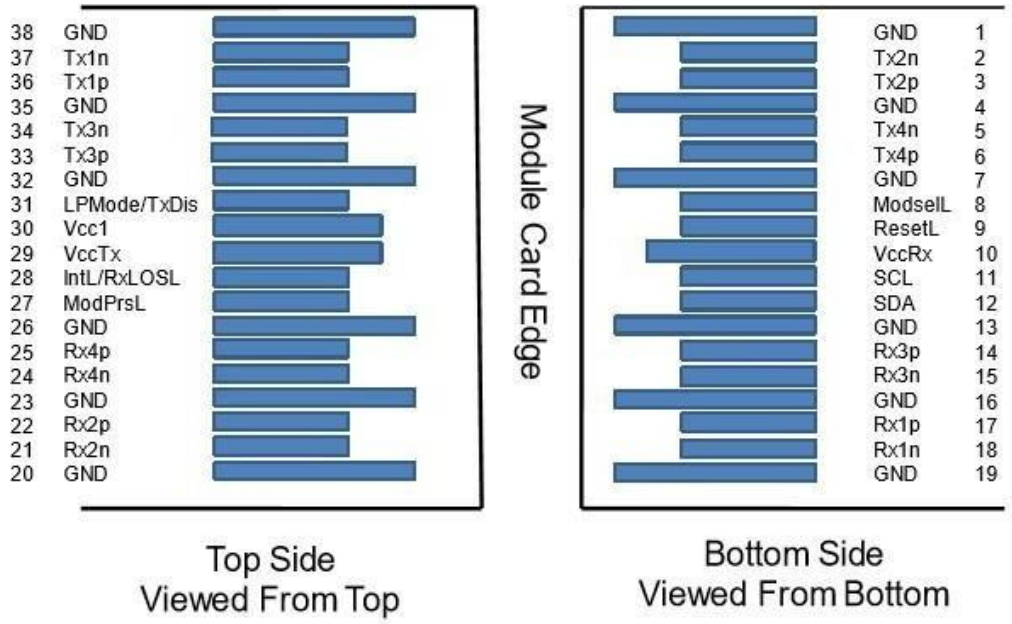


PIN	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B

28	LVTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A

57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69		Reserved	For Future Use	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

Pin Descriptions of QSFP28



PIN	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModselL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	

15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636). Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636).	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636).	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

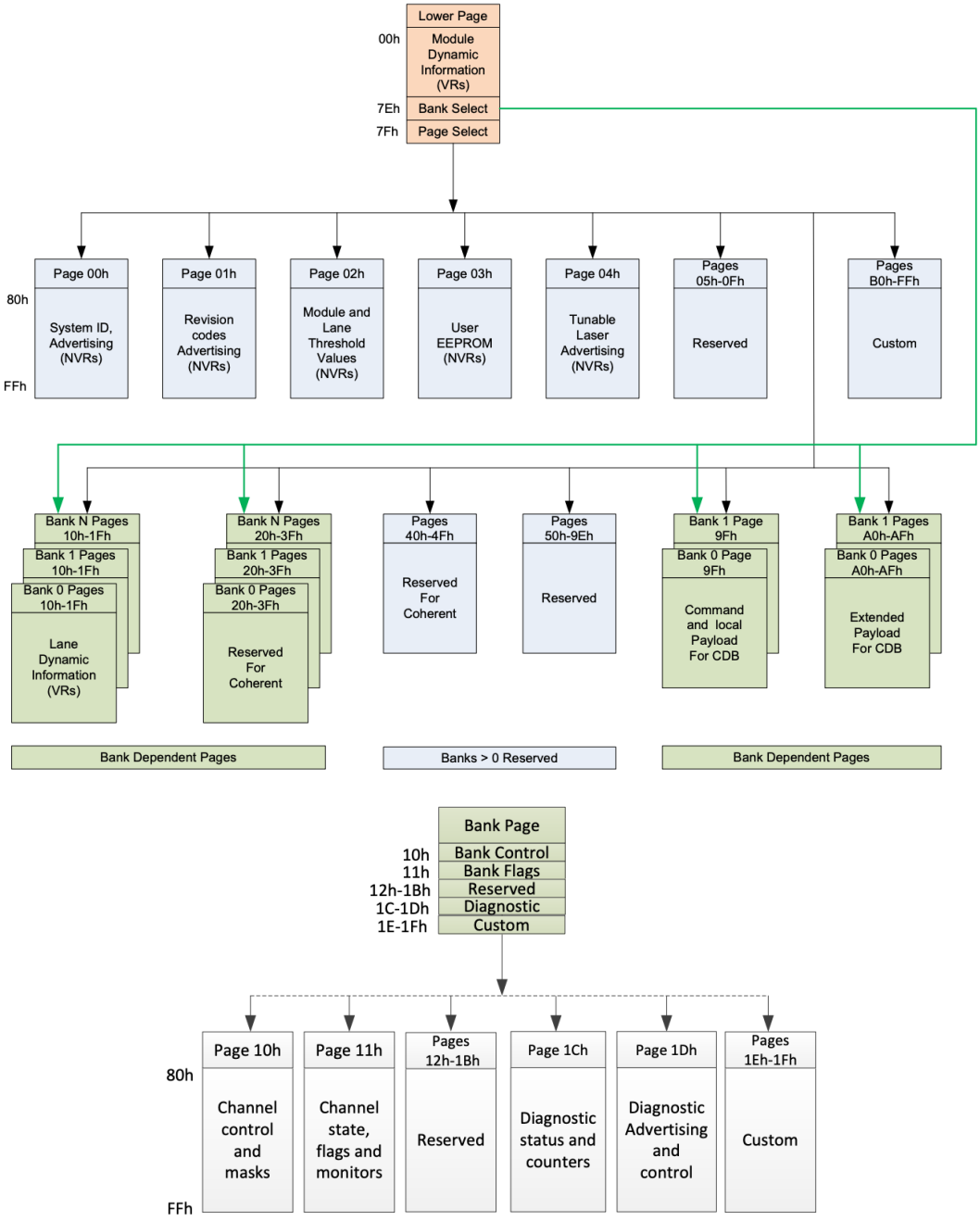
Notes:

1. GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board

signal common ground plane.

2. VccRx, Vcc1 and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1 A.

Memory Map (Compliant with QSFP-DD CMIS Rev4.0)



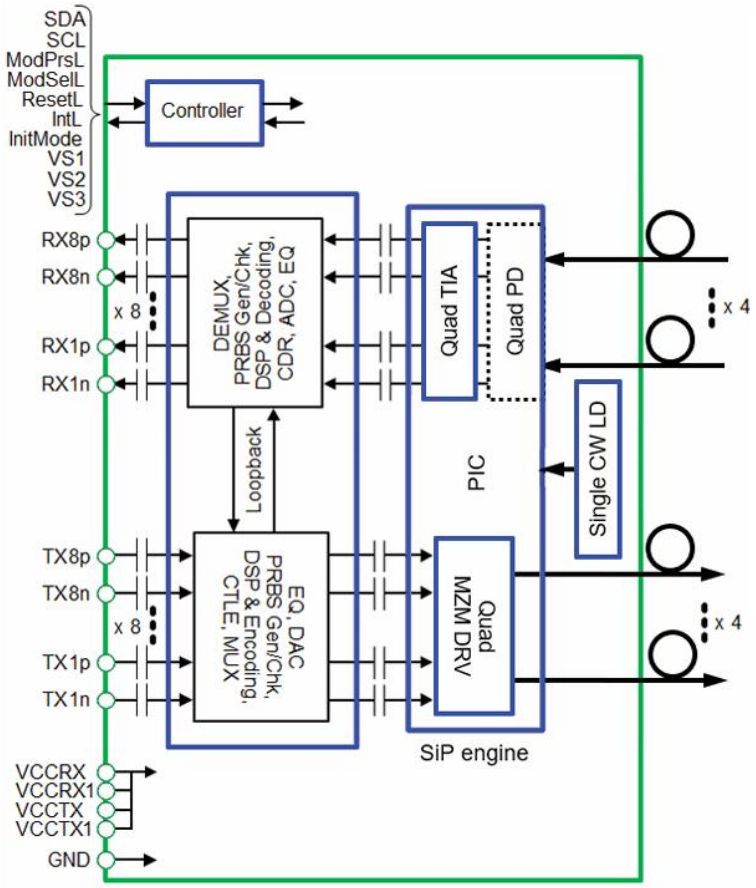
Memory map (Compliant withQSFP28 SFF-8636)

	2-Wire Serial Address 1010000x
	Lower Page 00h
0	Identifier
1-2	Status
3-21	Interrupt Flags
22-23	Free Side Device Monitors
34-81	Channel Monitors
82-85	Reserved
86-98	Control
99	Reserved
100-104	Hardware Interrupt Pin Masks
105-106	Vendor Specific
107	Reserved
108-110	Free Side Device Properties
111-112	Assigned for use by PCI Express
113	Free Side Device Properties
114-118	Reserved
119-122	Password Change Entry Area (Optional)
123-126	Password Entry Area (Optional)
127	Page Select Byte

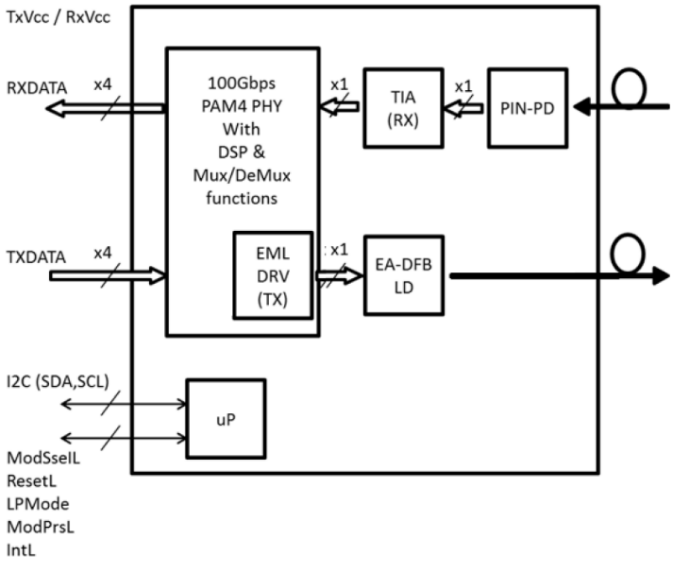
	Optional	Optional	Optional
Upper Page 00h	Page 01h	Page 02h	Page 03h
128 Identifier	128 CC_APPS	128-255 User EEPROM data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		
	130-131 Application Code Entry 0		
	132-133 Application Code Entry 1		
	134-253 other entries		176-223 Channel Thresholds
192-223 Extended ID			
224-255 Vendor Specific ID			224 TX EQ & RX Emphasis Magnitude ID
			225 RX output amplitude indicators
			226-241 Channel Monitor Masks
	254-255 Application Code Entry TL		252-255 Reserved

Recommended Host - Transceiver Interface Block Diagram

QSFP-DD SIDE



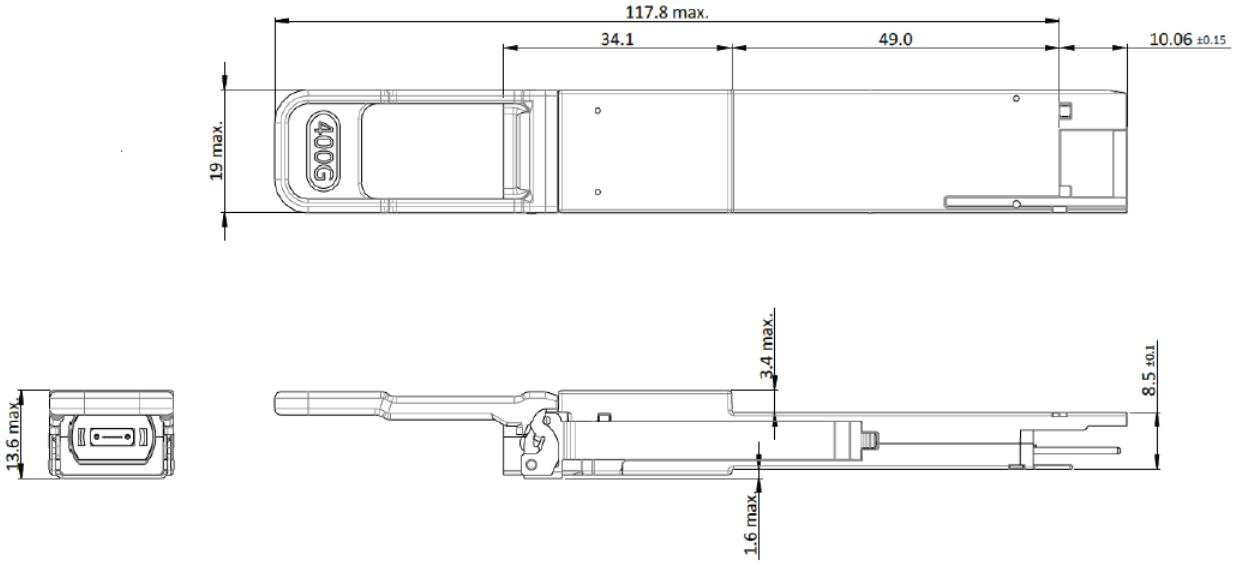
QSFP28 SIDE



Mechanical Drawing

a. QSFP-DD

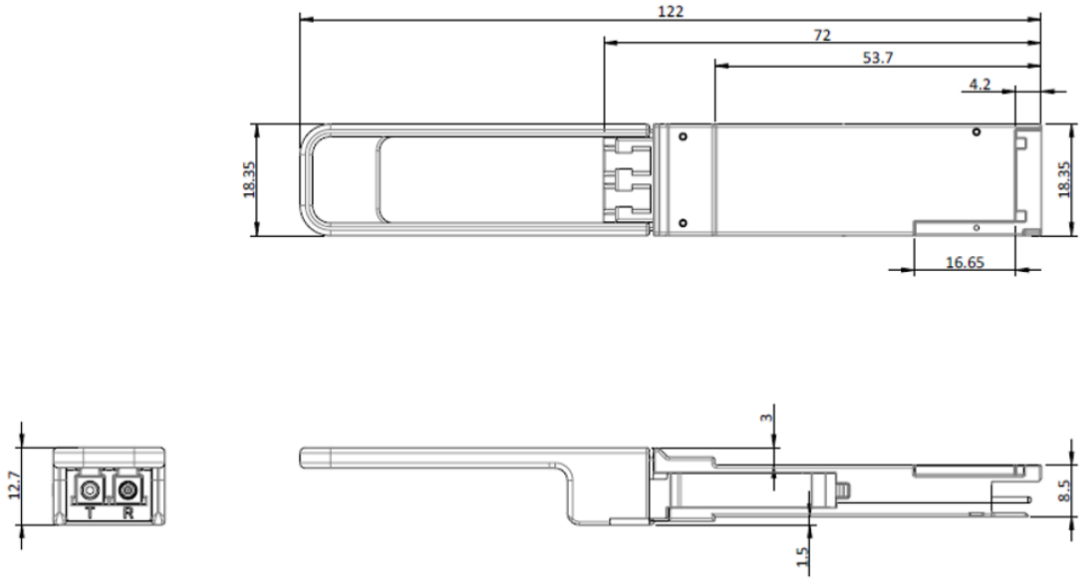
Unit: mm



Pull tab color: Yellow

b. QSFP

Unit: mm



Pull tab color: Yellow

c. Cable Length

Cable Length (Unit: meter)	Tolerant (Unit: cm)
＜1.0	+5/-0
1.0~4.5	+15/-0
5.0~14.5	+30/-0
≥15.0	+2%/-0

Ordering Information

Part No	Specification							
	Package	Data rate	Laser	Fiber	Cable Type	Cable Length	Temp.	Application
WS-D44Q-AOCLC019	QSFP-DD to QSFP28	400Gbps	1310nm	SMF	LSZH	1m	0~70°C	400GbE for 4x100G
WS-D44Q-AOCLC029	QSFP-DD to QSFP28	400Gbps	1310nm	SMF	LSZH	2m	0~70°C	400GbE for 4x100G
WS-D44Q-AOCLC039	QSFP-DD to QSFP28	400Gbps	1310nm	SMF	LSZH	3m	0~70°C	400GbE for 4x100G
WS-D44Q-AOCLC059	QSFP-DD to QSFP28	400Gbps	1310nm	SMF	LSZH	5m	0~70°C	400GbE for 4x100G
WS-D44Q-AOCLC079	QSFP-DD to QSFP28	400Gbps	1310nm	SMF	LSZH	7m	0~70°C	400GbE for 4x100G
WS-D44Q-AOCxCxx9	QSFP-DD to QSFP28	400Gbps	1310nm	SMF	LSZH OFNP, OFNR	xx m	0~70°C	400GbE for 4x100G

Note:

Cable type: x= L for LSZH, P for OFNP, R for OFNR, X for LSZH or OFNR or OFNP

Length: xx in meter

Variant Length and Cable Types can be customized. Please contact our sales for detail information

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	31-Dec-2024	New Issue	Ken Cheng	Joanne Ni	Tom Tang

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