WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

800G QSFP-DD 1311nm DR8 500m Transceiver
P/N: WST-QD8-DR8-C

Features:

- QSFP-DD form factor
- Supports a single 800 Gb/s aggregate data rate
- 8 x 100GBASE-DR optical interface
- 8 x 100GAUI-1 C2M electrical interface
- Compliant with QSFP-DD MSA HW Rev 6.01 type 2A with MPO-16/APC connector
- Two-wire serial interface with digital diagnostic monitoring (DDM)
- Power consumption: Typical 15 W, Max. 18 W
- Class 1 Laser
- Operating case temperature: Commercial: 0 ℃ to 70 ℃

Application:

- 800GBASE-DR8
- 800 Gigabit Ethernet links over single-mode fiber
- Supports 2 x 400 G, 4 x 200 G, and 8 x 100 G split modes for breakout applications, with partial link capability
- Data center interconnect
- Switch-to-switch and switch-to-router interconnections

Standard:

- Compliant with IEEE 802.3df
- Compliant with IEEE 802.3ck
- Compliant with CMIS Rev 5.0
- Complies with EU Directive 2011/65/EU (RoHS compliant)

Description

The module is an 800 Gb/s QSFP-DD optical transceiver designed for 500 m transmission over single-mode fiber (SMF). It provides eight electrical lanes and eight optical lanes operating at 106.25 Gb/s PAM4 signaling, supporting an aggregate data rate of 800 Gb/s. The module supports an 8 x 100GBASE-DR optical interface and an 8 x 100GAUI-1 C2M electrical interface. It integrates optical and electrical components within a QSFP-DD form factor and uses an MPO-16/APC connector for optical connectivity. The optical transmitters are based on 1311 nm EML technology, and the receivers use PIN photodiodes, optimized for high-speed single-mode fiber data center interconnect applications.

Function Description

The module converts 8 × 100GAUI-1 (53.125 GBd PAM4) C2M electrical input signals into optical outputs through integrated transmit circuitry and EML drivers, enabling 800 Gigabit Ethernet links over single-mode fiber. The optical interface consists of eight transmit and eight receive lanes through an MPO-16/APC connector. On the receive side, incoming optical signals are converted into electrical signals through PIN photodetectors and receiver circuitry. The electrical interface is compliant with 8 × 100GAUI-1 C2M, and the optical interface supports 8 × 100GBASE-DR operation up to 500 m over single-mode fiber. The module is intended for operation in systems that employ host-side KP4 forward error correction (FEC) to ensure reliable data transmission. The module supports digital diagnostic monitoring (DDM) through the two-wire serial interface compliant with CMIS Rev. 5.0.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	TS	-40	85	ºC	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Data Input Voltage Differential	$\lvert V_{DIP}-V_{DIN}\rvert$		1	V	
Control Input Voltage	VI	-0.3	VCC+0.5	V	
Control Output Current	IO	-20	20	mA	

Recommended Operating Environment

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TOPR	0		70	ºC	1
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Supply Current	ICC		4550	5742	mA	
Maximum Power Dissipation	PD		15	18	W	
Maximum Power Dissipation, Low Power Mode	PDLP			2.5	W	
Data Rate per Lane	DRL		106.25		Gb/s	
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3		VCC*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Instantaneous peak current at hot plug	ICC_IP			7200	mA	
Power Supply Noise 1 kHz - 1 MHz (p-p)				66	mVpp	
Operating Distance		2		500	m	

Electrical Specification High Speed Signal (compliant with IEEE802.3ck C2M)

Parameter		Symbol	Min.	Typical	Max.	Unit	Note
Transmitter Section:							
Differential pk-pk input Voltage tolerance (TP1a)			750			mV	
Peak-to-peak AC common-mode voltage tolerance	Low-frequency, VCMLF		32			mV	
	Full-band, VCMFB		80				
Differential-mode to common-mode return loss		RLcd	802.3ck 120G-2			dB	
Effective return loss		ERL	8.5			dB	
Differential termination mismatch					10	%	
Single-ended voltage tolerance range			-0.4		3.3	V	
DC common-mode voltage tolerance			-0.35		2.85	V	
Receiver Section:							
Peak-to-peak AC common-mode voltage	Low-frequency, VCMLF				32	mV	
	Full-band, VCMFB				80		
Differential peak-to-peak output voltage	Short mode				600	mV	
	Long mode				845		
Eye height		EH	15			mV	
Vertical eye closure		VEC			12	dB	
Common-mode to differential-mode return loss		RLDc	802.3ck 120G-1			dB	
Effective return loss		ERL	8.5			dB	
Differential termination mismatch					10	%	
Transition time			8.5			ps	
DC common-mode voltage tolerance			-0.35		2.85	V	

Electrical Specification Low Speed Control and Sense Signals (compliant with QSFP-DD HW Rev 6.01)

Parameter	Symbol	Min.	Max.	Unit	Note
Module output SCL and SDA	V_{OL}	0	0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3	VCC*0.3	V	
	V_{IH}	VCC*0.7	VCC+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	VCC+0.3	V	
IntL: Interrupt output, active low.	V_{OL}	0	0.4	V	
	V_{OH}	-	-	V	Host pull-up

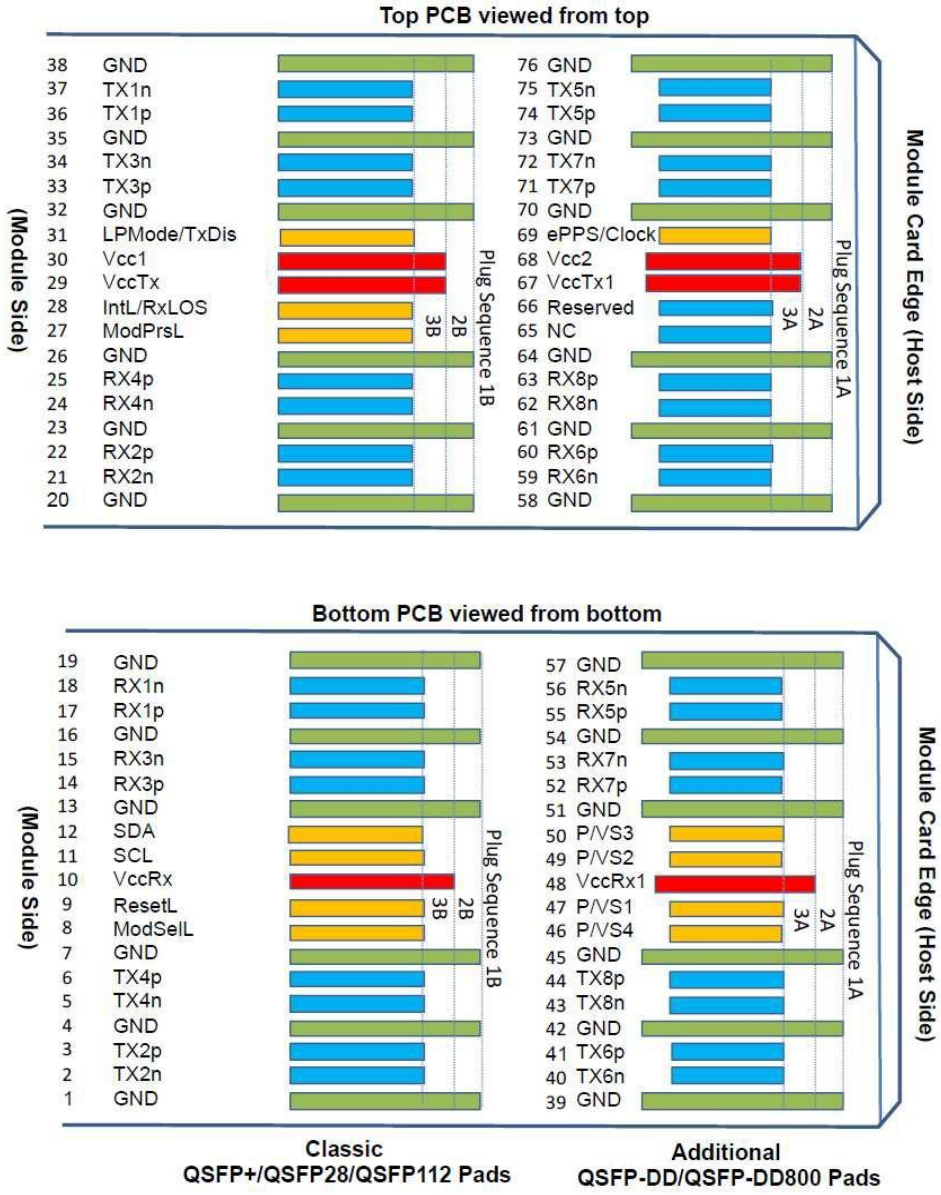
Optical Specifications

Parameter		Symbol	Min.	Typical	Max.	Unit	Note
Transmitter Section:							
Wavelength		λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio		SMSR	30			dB	
Average Launch Power, per lane		AOP_L	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMAouter), per Lane		T_{OMA}	-0.8		4.2	dBm	
Launch power in OMAouter minus TDECQ, per lane	for extinction ratio >= 5 dB	T_{OMA}-TDECQ	-2.2			dBm	
	for extinction ratio < 5 dB		-1.9				
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), per lane		TDECQ			3.4	dB	
TDECQ – 10log10(Ceq), per lane		Ceq			3.4	dB	
Average Launch Power of OFF Transmitter, per lane		T_{OFF}			-15	dBm	
Extinction Ratio		ER	3.5			dB	
Transmitter transition time		Tr			17	ps	
RIN15.5OMA		RIN			-136	dB/Hz	
Optical return loss tolerance		ORL			15.5	dB	
Transmitter Reflectance		T_R			-26	dB	2
Receiver Section:							
Wavelength		λ_{C0}	1304.5	1311	1317.5	nm	
Damage Threshold, per lane		AOP_D	5			dBm	
Average Receive Power, per lane		AOP_R	-5.9		4	dBm	
Receive Power (OMAouter), per lane		OMA_R			4.2	dBm	
Receiver Reflectance		RR			-26	dB	
Receiver Sensitivity (OMAouter), per lane		S_{OMA}			Max(–3.9, SECQ – 5.3)	dBm	3
Stressed Receiver Sensitivity (OMAouter), per lane		SRS			-1.9	dBm	4
Conditions of stressed receiver sensitivity test							
Stressed eye closure for PAM4 (SECQ), lane under test		SECQ		3.4		dB	
SECQ – 10log10(Ceq), lane under test		Ceq			3.4	dB	
OMAouter of each aggressor lane				4.2		dBm	

Notes:

1. Average launch power, per lane (min) is informative and not the principal indicator of signal strength
2. Transmitter reflectance is defined looking into the transmitter.
3. Receiver sensitivity (OMAouter), per lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB
4. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4}

Pin Assignment

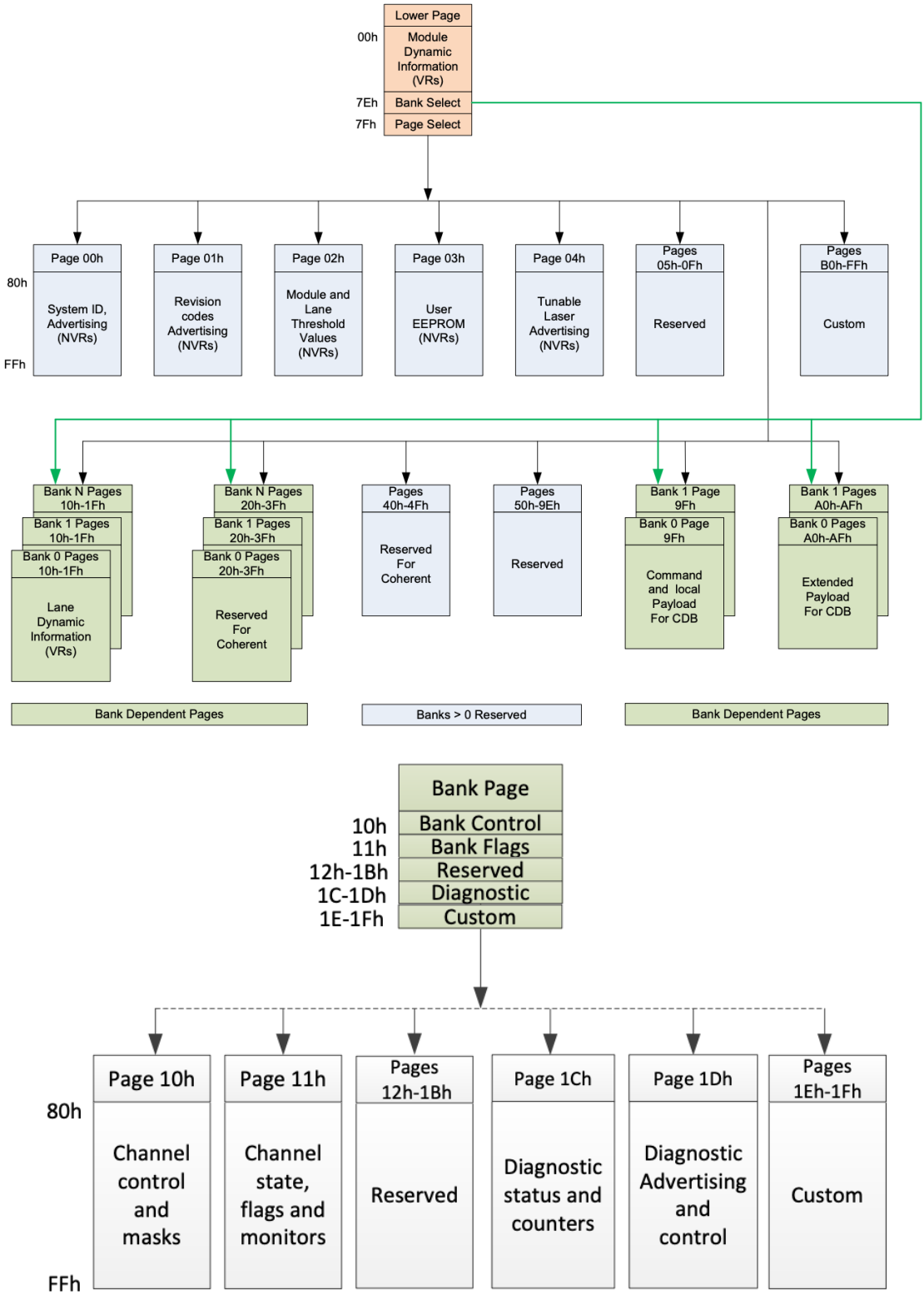


Pin Description

PIN #	Logic	Symbol	Definition	PIN #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46	LVCMOS/CML- I	P/VS4	Programmable/Module Vendor Specific 4

9	LVTTL-I	ResetL	Module Reset	47	LVCMO S /CML-I	P/VS1	Programmable/Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS -I/O	SCL	TWI serial interface clock	49	LVCMO S /CML-O	P/VS2	Programmable/Module Vendor Specific 2
12	LVCMOS -I/O	SDA	TWI serial interface data	50	LVCMO S /CML-O	P/VS3	Programmable/Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	69	LVCMO S-I	ePPS / Clock	1PPS PTP clock or reference clock input
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

QSFP-DD Module EEPROM Information and Management

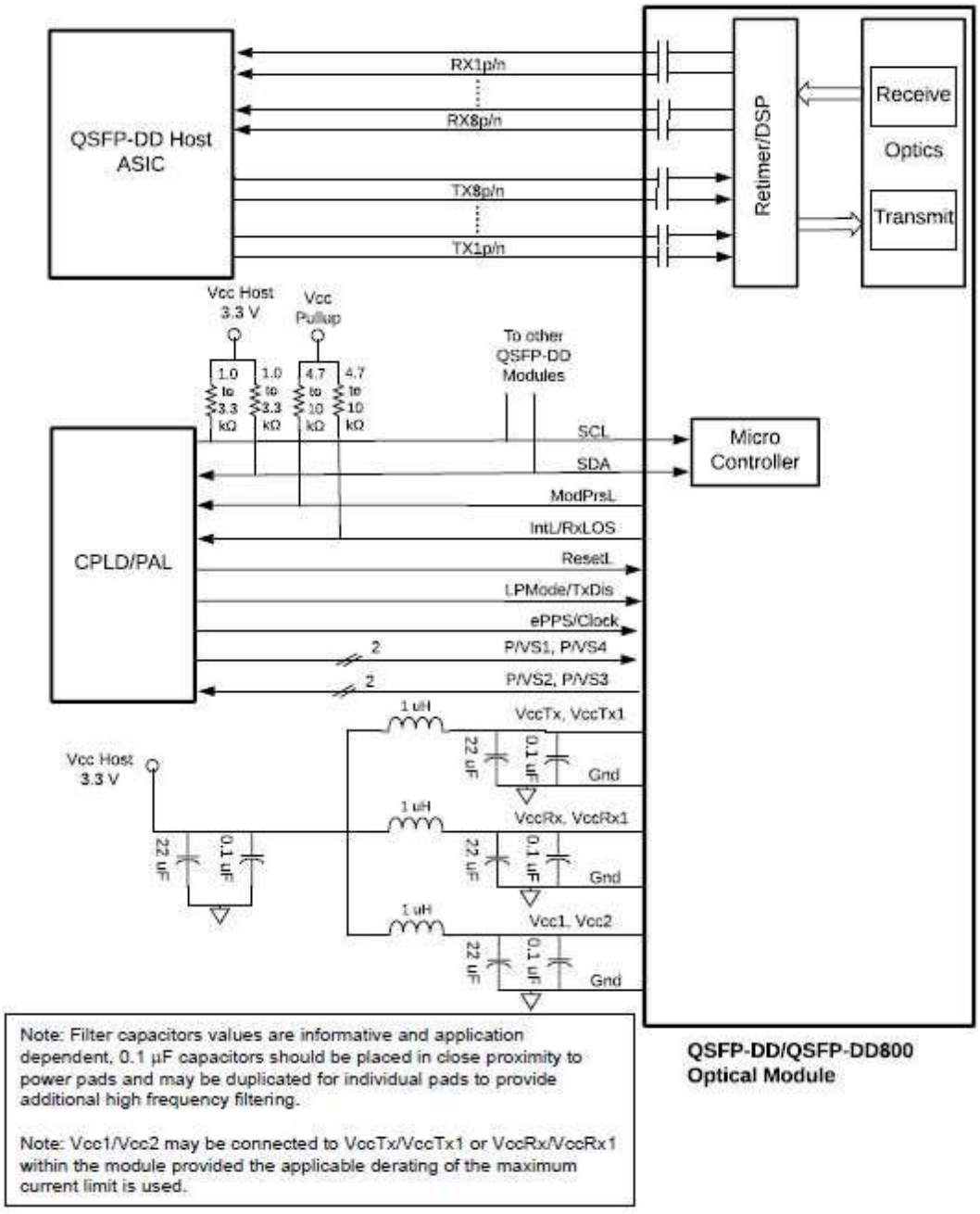


Digital Diagnostic Functions and Control and Status I/O Timing Characteristics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal

Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current (Per lane)	0 to 100	10%	mA	Internal
Tx Output Power (Per lane)	-2.9 to +4	±3	dB	Internal
Rx Receive Power (Per lane)	-5.9 to +4	±3	dB	Internal

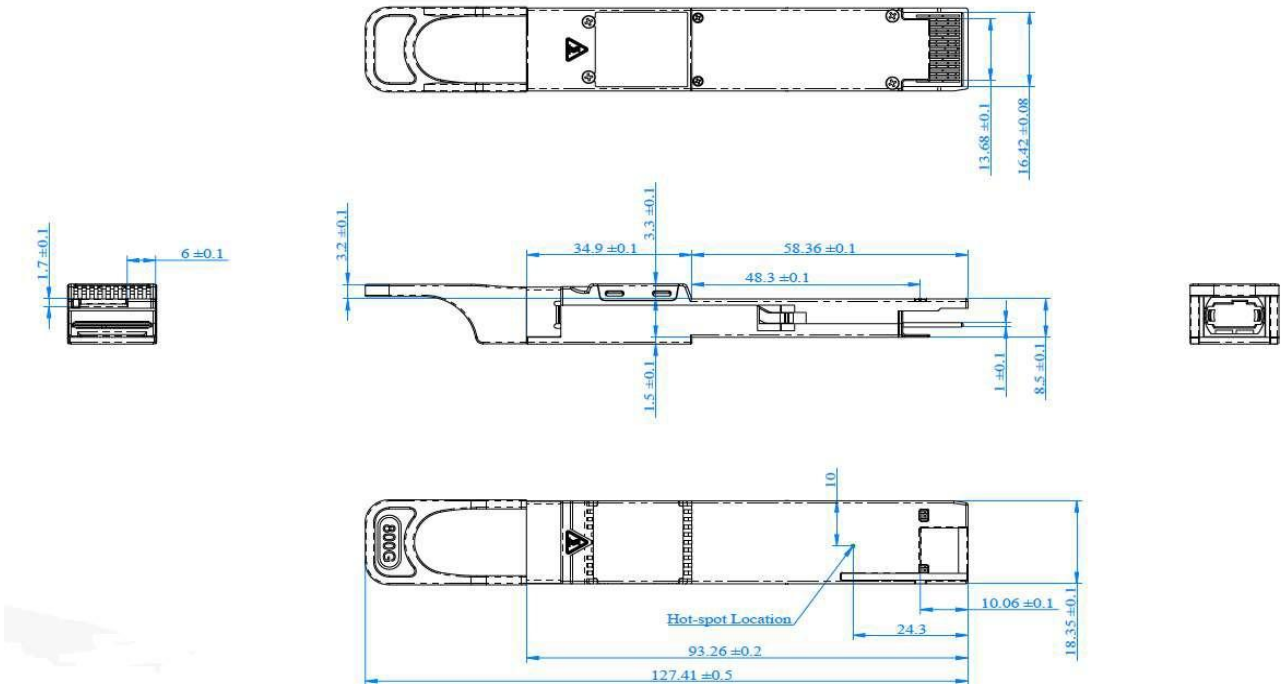
Recommended Circuit Diagram



Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

Mechanical Design Diagram



Unit: mm (All dimension are ±0.1mm, unless specified)

Ordering Information

Part No	Specification							
	Package	Data rate	Laser	Detector	Temp.	Reach	Other	Application code
WST-QD8-DR8-C	QSFP-DD	800 Gb/s	1311 nm EML	PIN	0 ~ 70 °C	500 m	DDM RoHS	800G Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	14-Apr-2023	New Issue	Ken Cheng	Wayne Liao	Tom Tang
V1.1	20-Oct-2025	Add photo and update layout	Amy Lee	Wayne Liao	Tom Tang
V1.2	8-Apr-2026	Update descriptions, typical power consumption and split mode, correct typos	Amy Lee	Wayne Liao	Tom Tang

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