WAVESPLITTER™
TECHNOLOGIES, INC.

Data Sheet

800G QSFP-DD 2xDR4 500m Transceiver

P/N: WST-QD8-DR4X2-C

Features:

- Supports 800Gb/s aggregate data rate via dual 400GBASE-DR4 interfaces
- 8 × 106.25 Gb/s PAM4 electrical lanes (53.125 GBaud)
- Compliant with QSFP-DD MSA HW Rev 7.0, Type 2B
- Dual MPO-12/APC optical interfaces for parallel single-mode fiber (SMF)
- Based on 1311 nm EML transmitter and PIN receiver
- Transmission distance up to 500 m over SMF
- Supports KP4 FEC (host-side) for error-free operation
- Power consumption: Typical 15.5 W, Max. 18 W
- Single 3.3 V power supply
- Hot-pluggable QSFP-DD form factor
- Supports digital diagnostics monitoring (DDM) via CMIS interface
- Operating case temperature: 0°C to 70°C
- RoHS compliant

Applications:

- 800G Ethernet links
- 2 × 400G Ethernet breakout applications (2 x DR4)
- Data center interconnect (DCI) up to 500 m
- High-performance computing (HPC) networks
- Cloud and hyperscale data center networks

Standards:

- QSFP-DD MSA HW Rev 7.0 (Type 2B)
- CMIS Rev 5.0
- IEEE 802.3cu-2021 (100GBASE-DR)
- IEEE 802.3bs-2017 (400GBASE-DR4)
- IEEE 802.3ck-2022 (100GAUI-1 / 400GAUI-4)
- IEEE 802.3-2018 Clause 91 (KP4 FEC)

Description

The WST-QD8-DR4X2-C is a hot-pluggable optical transceiver module in the QSFP-DD form factor, designed for 800 Gb/s Ethernet applications. The module integrates two independent 400GBASE-DR4 optical interfaces, each paired with a corresponding 400GAUI-4 electrical interface, enabling operation as either a single 800G link or two independent 400G links.

Each optical interface consists of four parallel lanes operating at 53.125 GBaud PAM4 (106.25 Gb/s per lane) over single-mode fiber (SMF). The module utilizes 1311 nm EML transmitters and PIN photodiode receivers, supporting transmission distances of up to 500 m via dual MPO-12/APC optical connectors.

The module is compliant with QSFP-DD MSA and relevant IEEE 802.3 standards, and is designed for use in systems employing host-side KP4 FEC to achieve reliable link performance.

Function Description

The module implements a dual-channel architecture, where each channel functions as an independent 400GBASE-DR4 optical interface.

On the electrical side, the host provides eight 100G PAM4 lanes (800GAUI-8), which are internally mapped into two groups of four lanes, corresponding to two independent 400GAUI-4 interfaces. Each group is processed through high-speed signal conditioning circuitry and drives a 4-lane optical transmitter.

On the transmit path, each lane is modulated using a 1311 nm EML, generating parallel optical signals that are coupled into single-mode fiber through dual MPO-12/APC connectors. On the receive path, incoming optical signals are detected by PIN photodiodes with integrated TIAs, converted into electrical signals, and delivered to the host as differential outputs.

The module includes an embedded controller that supports CMIS-compliant management, enabling digital diagnostics monitoring (DDM), status reporting, and control functions via a two-wire interface.

For reliable operation, the host system is required to implement KP4 FEC, as defined in IEEE 802.3, to compensate for channel impairments and ensure target bit error rate performance.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	85	ºC	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Data Input Voltage Differential	$\lvert V_{DIP}-V_{DIN}\rvert$	-	1	V	
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V	
Control Output Current	I_O	-20	20	mA	
Receiver Damage Threshold, each Lane	AOP_D	5	-	dBm	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TOPR	0	-	70	ºC	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Sustained peak current at hot plug	ICC_SP	-	4700	5741	mA	
Maximum Power Dissipation	PD	-	15.5	18	W	
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	2.5	W	
Signaling Speed per Lane	DRL	-	53.125	-	GBd	
Control Input Voltage High	VIH	VCC*0.7	-	VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3	-	VCC*0.3	V	
Instantaneous peak current at hot plug	ICC_IP	-	-	6600	mA	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Pre-FEC Bit Error Ratio				2.4 x 10-4		
Post-FEC Bit Error Ratio				1 x 10-12		1
Operating Distance	-	2	-	500	m	2

Notes:

1. KP4 FEC provided by host system.
2. KP4 FEC required on host system to support maximum distance.

Electrical Characteristics

Electrical Specification High Speed Signal (compliant with IEEE802.3ck C2M)

Receiver (Module Output, TP4)						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB	-	-	-	32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode	-	-	-	600 845	mV	
Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	

Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Transition time	-	8.5	-	-	ps	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
Transmitter (Module Input, TP1)						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	mV	
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB	-	32 80	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	

Electrical Specification Low Speed Control and Sense Signals (compliant with QSFP-DD HW Rev 6.01 Table 14)

Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Condition**
Module output SCL and SDA	V_{OL}	0	0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	V_{CC}+0.3	V	
IntL	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V	

Optical Characteristics

Transmitter Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength	λC	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power, each lane	AOPL	-2.9	-	4.0	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane	TOMA	-0.8	-	4.2	dBm	
Launch power in OMAouter minus TDECQ, each lane for extinction ratio >= 5 dB for extinction ratio < 5 dB	TOMA-TDECQ	 -2.2 -1.9	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
TDECQ – 10log10(Ceq), each lane	Ceq	-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-15	dBm	
Extinction Ratio	ER	3.5	-	-	dB	
Transmitter transition time	Tr			17	ps	
RIN15.5OMA	RIN	-	-	-136	dB/Hz	
Optical return loss tolerance	ORL	-	-	15.5	dB	
Transmitter Reflectance	TR	-	-	-26	dB	2

Notes:

1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength.

2: Transmitter reflectance is defined looking into the transmitter.

Receiver Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength	λCR	1304.5	1311	1317.5	nm	
Average Receive Power, each Lane	AOPR	-5.9	-	4	dBm	
Receive Power (OMAouter), each Lane	OMAR	-	-	4.2	dBm	
Receiver Reflectance	RR	-	-	-26	dB	

Receiver Sensitivity (OMAouter), each Lane	S_{OMA}	-	-	Max(–3.9, SECQ - 5.3)	dBm	1
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-1.9	dBm	2
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	-	3.4	-	dB	
SECQ – 10log10(Ceq), lane under test	Ceq	-	-	3.4	dB	
OMAouter of each aggressor lane	-	-	4.2	-	dBm	

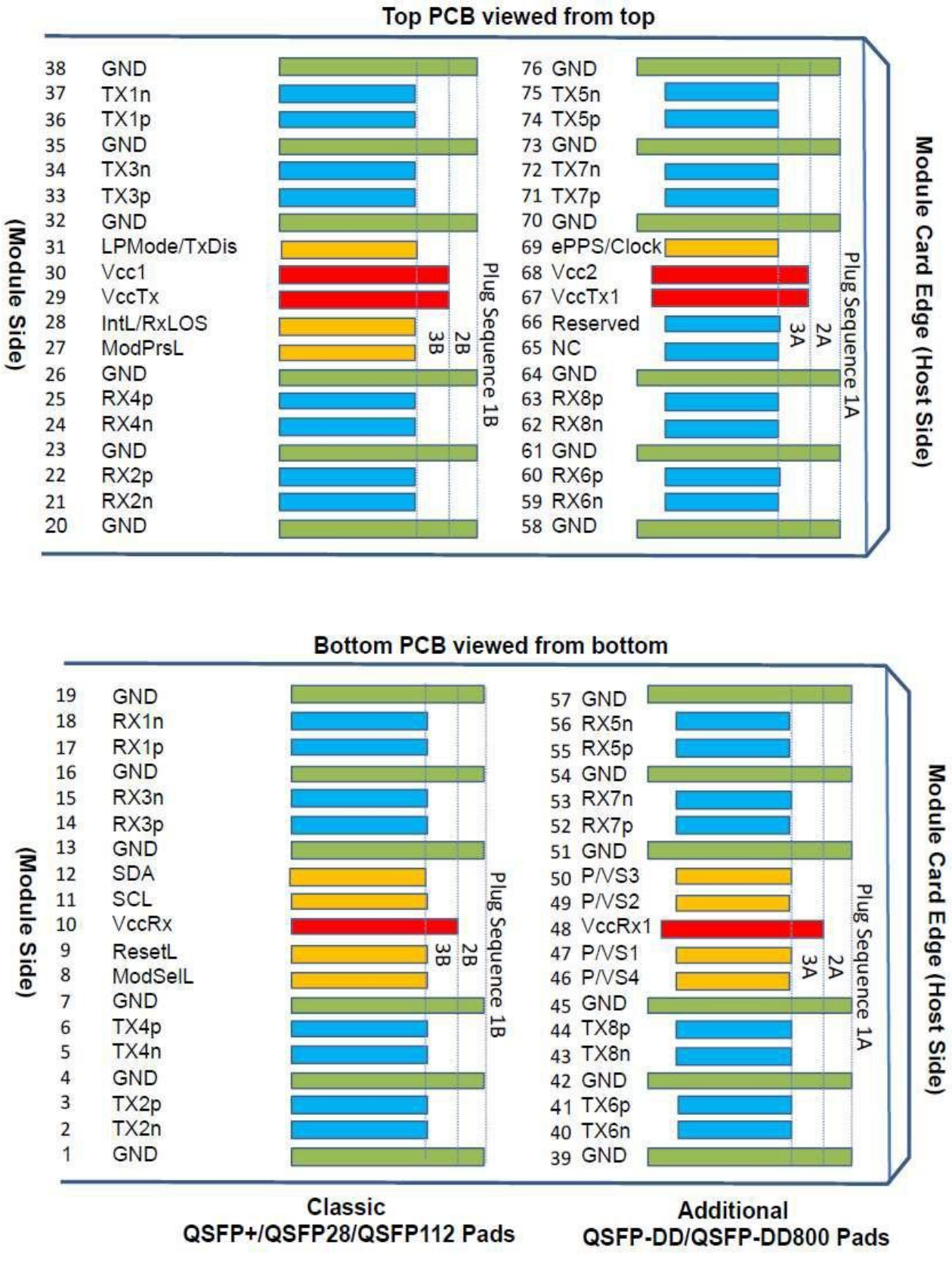
Note:

1. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
2. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4}

Digital Diagnostic Functions and Control and Status I/O Timing Characteristics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-2.9 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-5.9 to +4	±3	dB	Internal

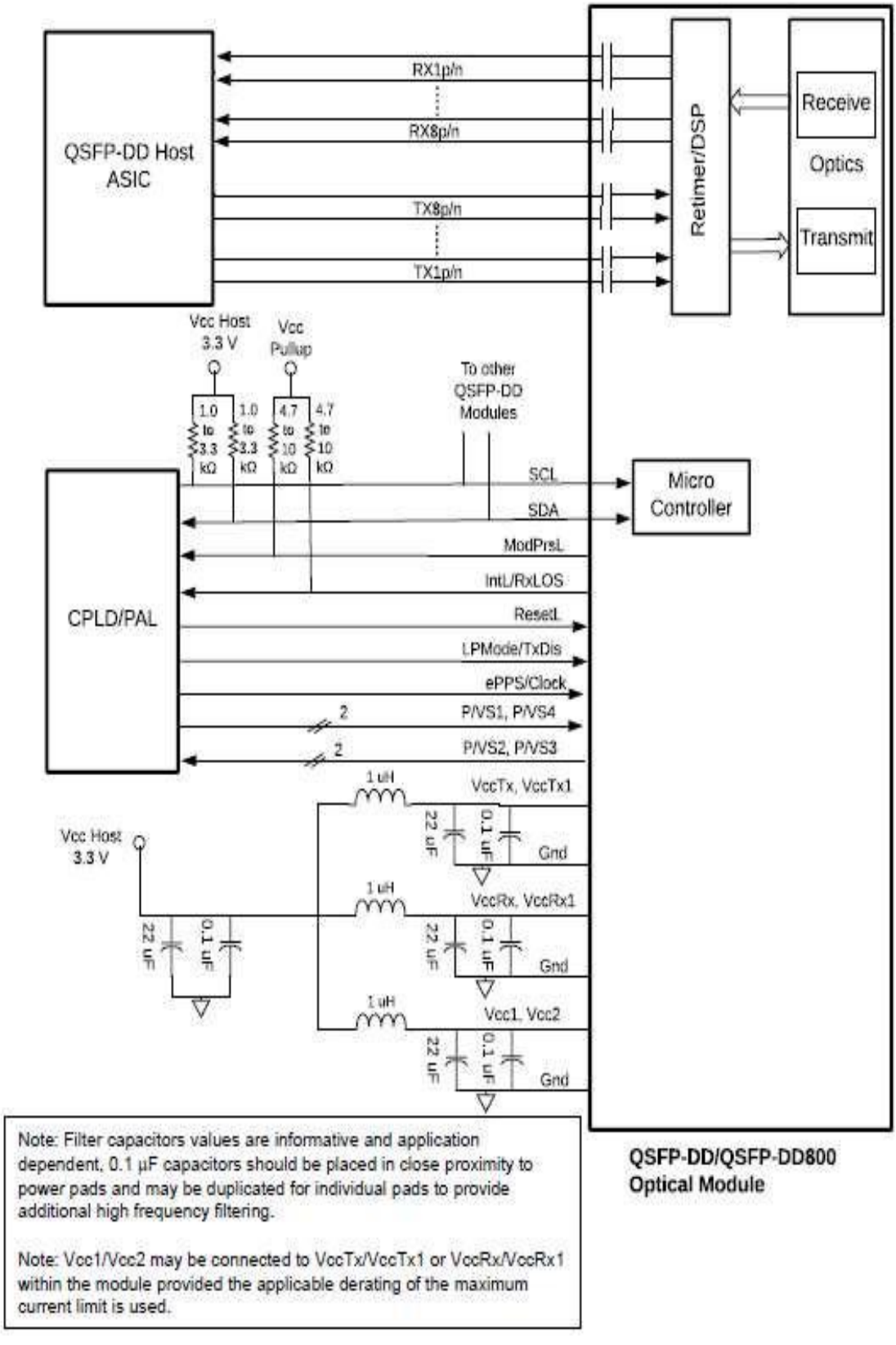
Pin Assignment



Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46	LVCMOS /CML-I	P/VS4	Programmable/Module Vendor Specific 4
9	LVTTL-I	ResetL	Module Reset	47	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS -I/O	SCL	TWI serial interface clock	49	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2
12	LVCMOS -I/O	SDA	TWI serial interface data	50	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground

20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	69	LVCMOS-I	ePPS /Clock	1PPS PTP clock or reference clock input
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

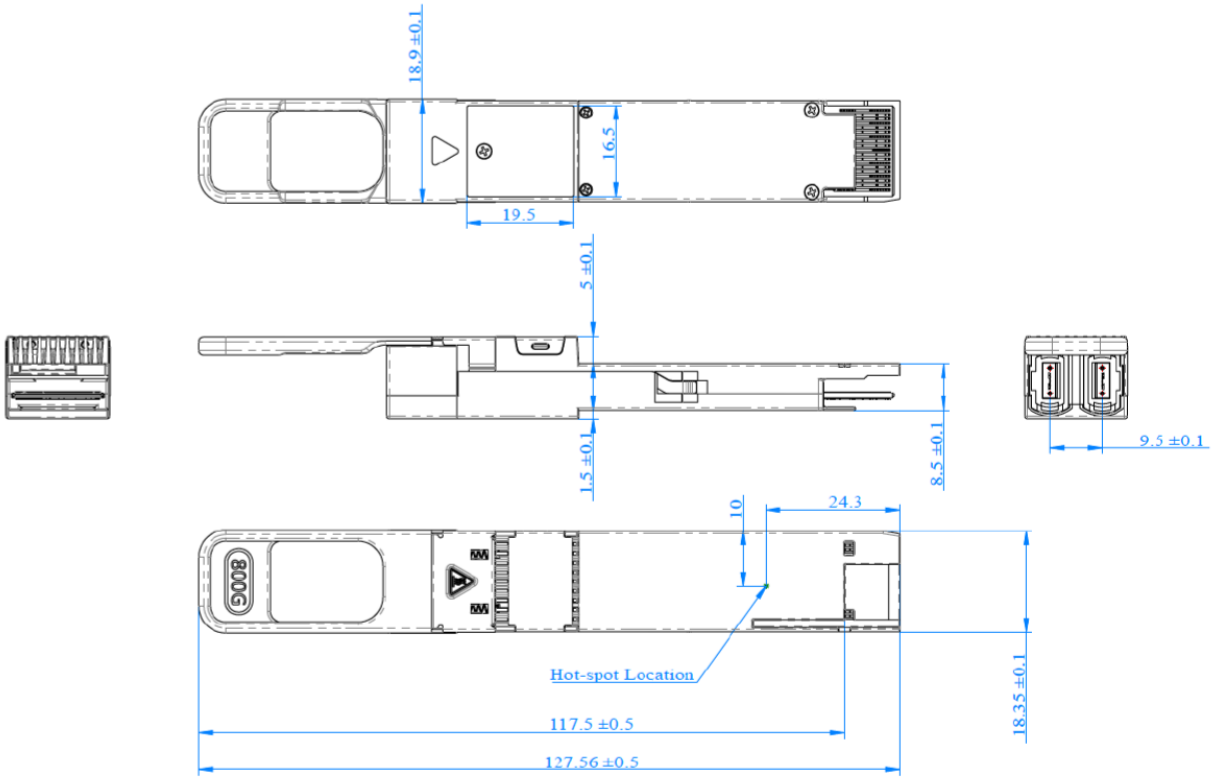
Host Board Schematic



Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification							
	Package	Data rate	Laser	Detector	Temp	Reach	Other	Application code
WST-QD8-DR4X2-C	QSFP-DD	800 Gbps	1311nm-EML	PIN	0 ~ 70 °C	500m	DDM RoHS	800G Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	15-Sep-2025	New Issue	Kai-Hsu Cheng	Wayne Liao	Wayne Liao
V1.1	20-Dec-2025	Update mechanical drawing	Henry Chen	Wayne Liao	Tom Tang

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