Data Sheet

800G QSFP-DD 2xSR4 Transceiver Module
P/N: WST-QD8-SR4X2-C

Features:

- QSFP-DD form factor
- Supports a single 800 Gb/s aggregate data rate
- 8 × 106.25 Gb/s PAM4 optical interface
- 8 × 106.25 Gb/s PAM4 electrical interface
- Eight-channel parallel VCSEL transmitters and PIN photodiode receivers with TIAs
- Dual MPO-12/APC optical connector
- 2xSR4 (100 m) optical interface over OM4 multimode fiber with host-side KP4 FEC
- Hot pluggable
- Single 3.3 V power supply
- Power consumption: Typical 12.5 W, Max. 15 W
- Operating case temperature: 0 °C to +70 °C
- Digital diagnostic monitoring support

Applications:

- 800 Gigabit Ethernet or InfiniBand links over multimode fiber
- Supports 2 x 400 G, 4 x 200 G, and 8 x 100 G split modes for breakout applications, with partial link capability.
- Data center interconnect applications
- Switch-to-switch and switch-to-router

Standards:

- IEEE 802.3db and IEEE 802.3df compliant
- IEEE 802.3ck compliant
- QSFP-DD MSA compliant
- CMIS management interface compliant with CMIS 5.0
- RoHS compliant

Description

The module is an 800 Gb/s QSFP-DD optical transceiver designed for short-reach multimode fiber (MMF) transmission. It provides eight electrical lanes operating at 106.25 Gb/s PAM4 signaling and supports a 2xSR4 optical interface for transmission distances up to 100 m over OM4 multimode fiber.

The module integrates optical and electrical components within a QSFP-DD form factor and uses an MPO-12/APC connector for optical connectivity. The optical transmitters are based on 850 nm VCSEL technology and the receivers use PIN photodiodes, optimized for short-reach multimode fiber applications.

Functional Description

The module converts 8 × 106.25 Gb/s PAM4 electrical input signals into optical outputs through integrated transmit circuitry and VCSEL laser drivers, enabling 800 Gigabit Ethernet links over multimode fiber. The optical interface consists of eight transmit and eight receive lanes using an MPO-12/APC connector. On the receive side, incoming optical signals are converted into electrical signals through PIN photodetectors and receiver circuitry. The module is intended for operations in systems that employ host-side KP4 forward error correction (FEC) to ensure reliable data transmission.

The module supports digital diagnostic monitoring (DDM) through the QSFP-DD management interface, enabling monitoring of key operating parameters.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	TS	-40	85	°C	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity	RH	5	85	%	Non-condensation
Receiver Damage Threshold (per lane)	R_D		+5	dBm	1

Note 1: This parameter defines the maximum optical input power the receiver can withstand without damage and is not an operating condition.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Electrical Signal Rate (per lane)		53.125 ± 100 ppm			GBd	
Optical Signal Rate (per lane)		53.125 ± 100 ppm			GBd	
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Operating Case Temperature	T_C	0		70	°C	
Power Consumption	P_C		12.5	15	W	
Supply Current	Icc		3790	4785	mA	
Link Distance (OM4)	DI	0.5		100	m	

Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Test Point	Min	Typ	Max	Unit	Note
High Speed Electrical Input Characteristics						
Signaling rate (per lane)	TP1	53.125 ± 100 ppm			GBd	
Differential pk-pk input voltage tolerance	TP1a	750			mV	
AC common-mode RMS voltage	TP1a	25			mV	
Single-ended voltage tolerance	TP1a	-400		3300	mV	
DC common-mode voltage	TP1	-350		2850	mV	

High Speed Electrical Output Characteristics						
Signaling rate (per lane)	TP4	53.125 ± 100 ppm			GBd	
AC common-mode output voltage (RMS)	TP4			25	mV	
Differential peak-to-peak output voltage	TP4				mV	
Short mode				600		
Long mode				845		
Eye height	TP4	15			mV	
DC common-mode voltage	TP4	-350		2850	mV	

Optical Characteristics (Under Recommended Operating Conditions)

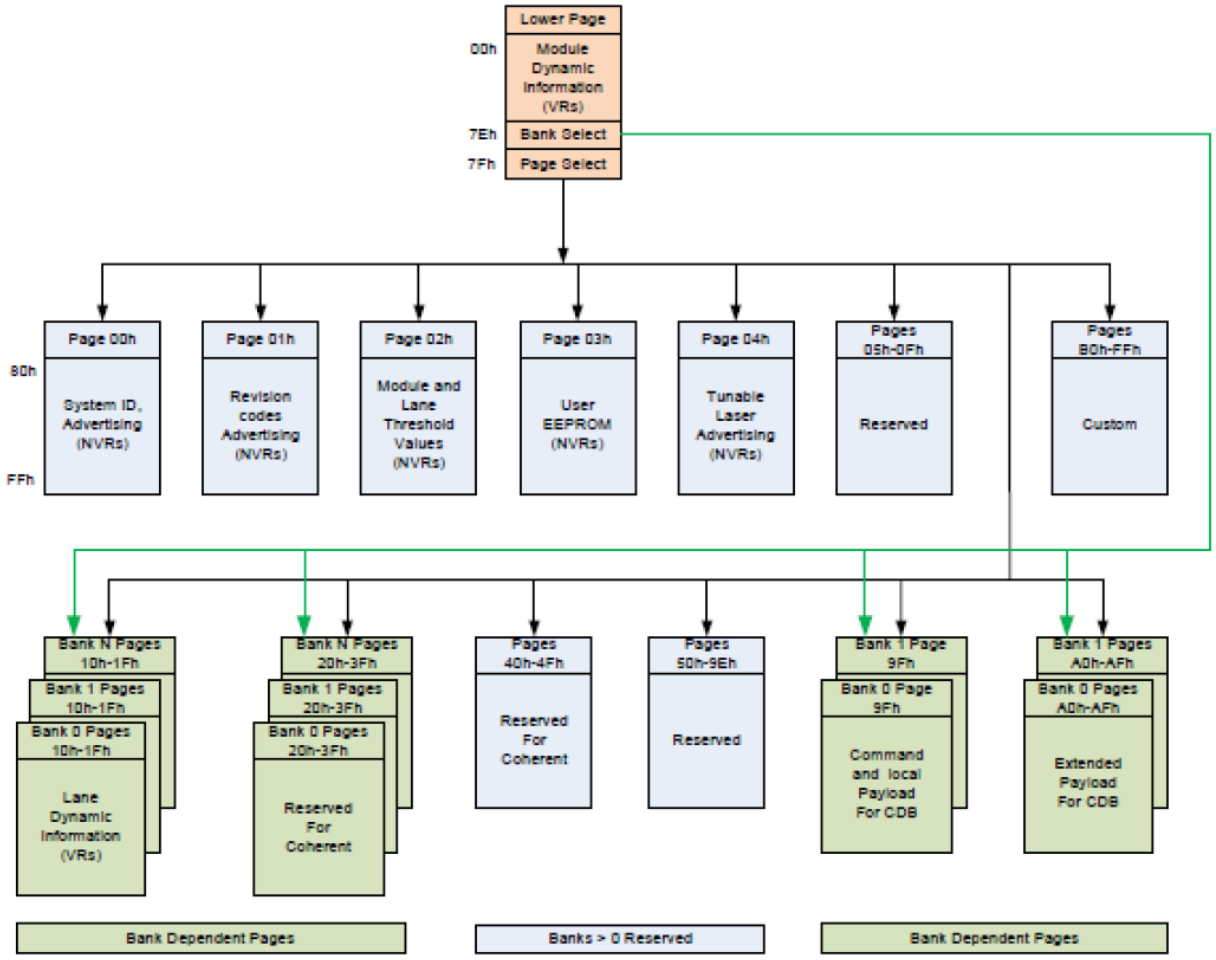
Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Signaling speed (per lane)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths	λ	840		870	nm	
RMS spectral width				0.65	nm	1
Average launch power (per lane)	P	-4.6		4	dBm	2
OMAouter (per lane)	P_{OMA}				dBm	2, 3
For max (TECQ, TDECQ) ≤ 1.8 dB		-2.6		3.5		
For 1.8 < max (TECQ, TDECQ) ≤ 4.4 dB		-4.4 + max (TECQ, TDECQ)		3.5		
Transmitter and dispersion eye closure for PAM4 (TDECQ) (per lane)				4.4	dB	
Transmitter eye closure for PAM4 (TECQ) (per lane)				4.4	dB	
Extinction ratio (per lane)	ER	2.5			dB	
Average launch power of OFF transmitter (per lane)	P_{off}			-30	dBm	
$RIN_{21}OMA$	RIN			-132	dB/Hz	
Optical return loss tolerance				14	dB	
Encircled flux		≥ 86 % at 19 μm ≤ 30 % at 4.5 μm				4
Receiver						
Signaling speed (per lane)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane Wavelengths	λ	840		870	nm	
Average receive power (per lane)		-6.4		4	dBm	2, 5
Receive power (OMAouter) (per lane)	R_{OMA}			3.5	dBm	

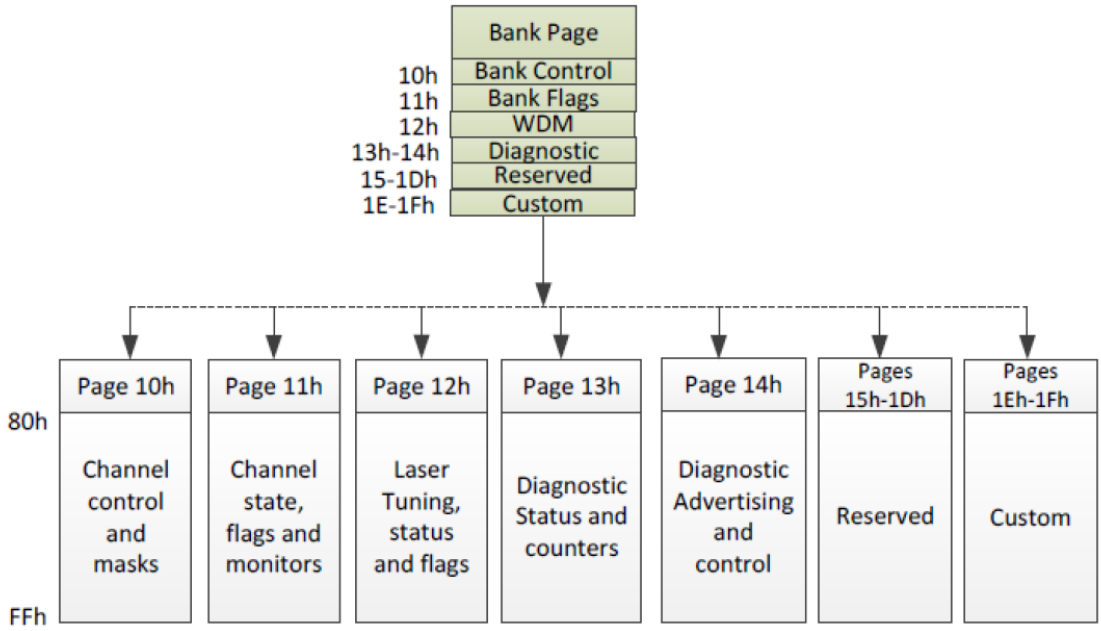
Receiver Reflectance				-15	dB	
Receiver sensitivity (OMAouter) (per lane)	SEN	max(-4.4, SECQ-6.4)			dBm	6
LOS Assert		-15			dBm	
LOS De-Assert				-6.6	dBm	
LOS Hysteresis		0.5			dB	
Conditions of stressed receiver sensitivity test:						7
Stressed eye closure for PAM4 (SECQ), lane under test		4.4			dB	
OMAouter of each aggressor lane		3.5			dBm	

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Receiver sensitivity is defined based on stressed receiver conditions per IEEE 802.3.
3. Even if the TDECQ <1.4 dB, the OMA (min) must exceed this value.
4. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 µm fiber, in accordance with IEC 61280-1-4.
5. Average receive power, per lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.4 dB.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

MEMORY MAP (compliant with CMIS Rev. 5.0)

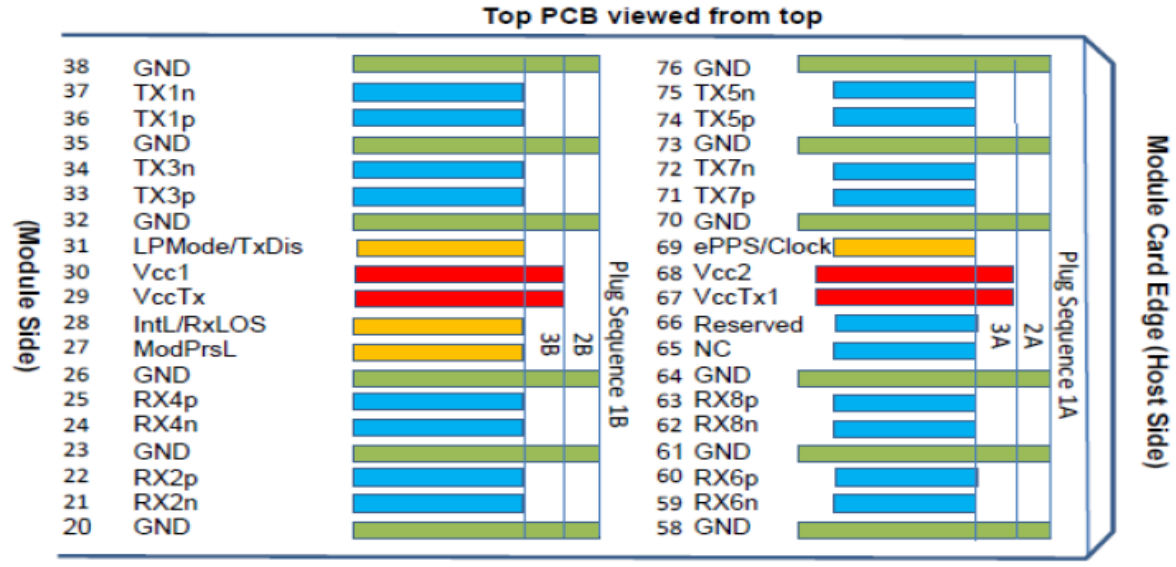


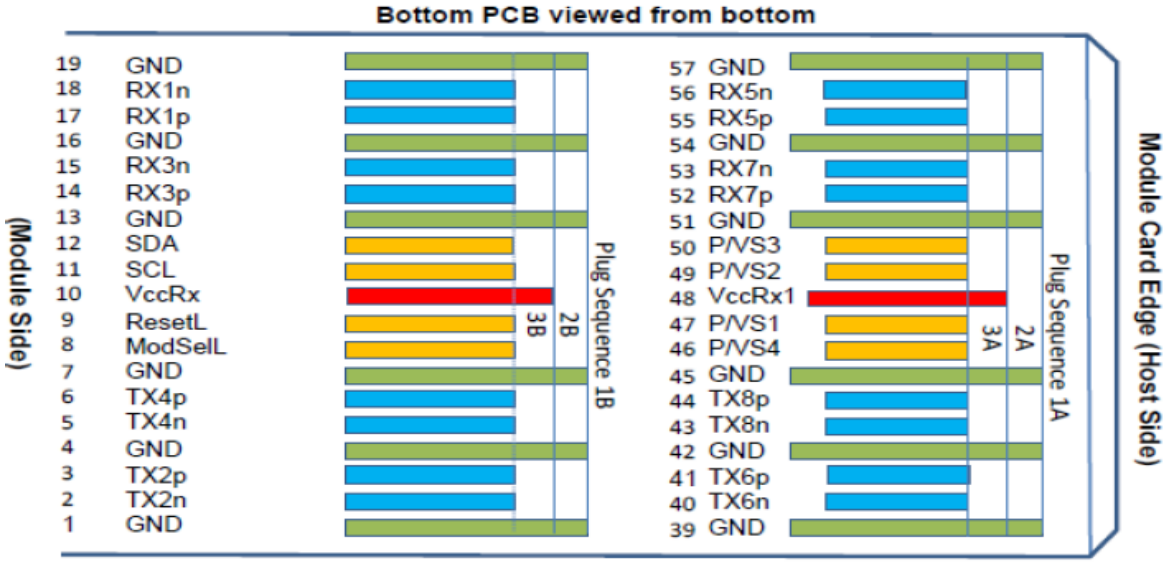


Digital Diagnostic Monitoring Functions (Under Recommended Operating Conditions)

Parameter	Accuracy	Unit	Note
Measured transceiver case temperature	±3	°C	
Measured transceiver supply voltage	±3	%	
Measured Tx bias current	±10	%	
Measured Tx output power	±3	dB	
Measured Rx received average optical power	±3	dB	

Pin Assignment





Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		$V_{CC}Rx$	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		$V_{CC}Tx$	+3.3 V Power Supply Transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	

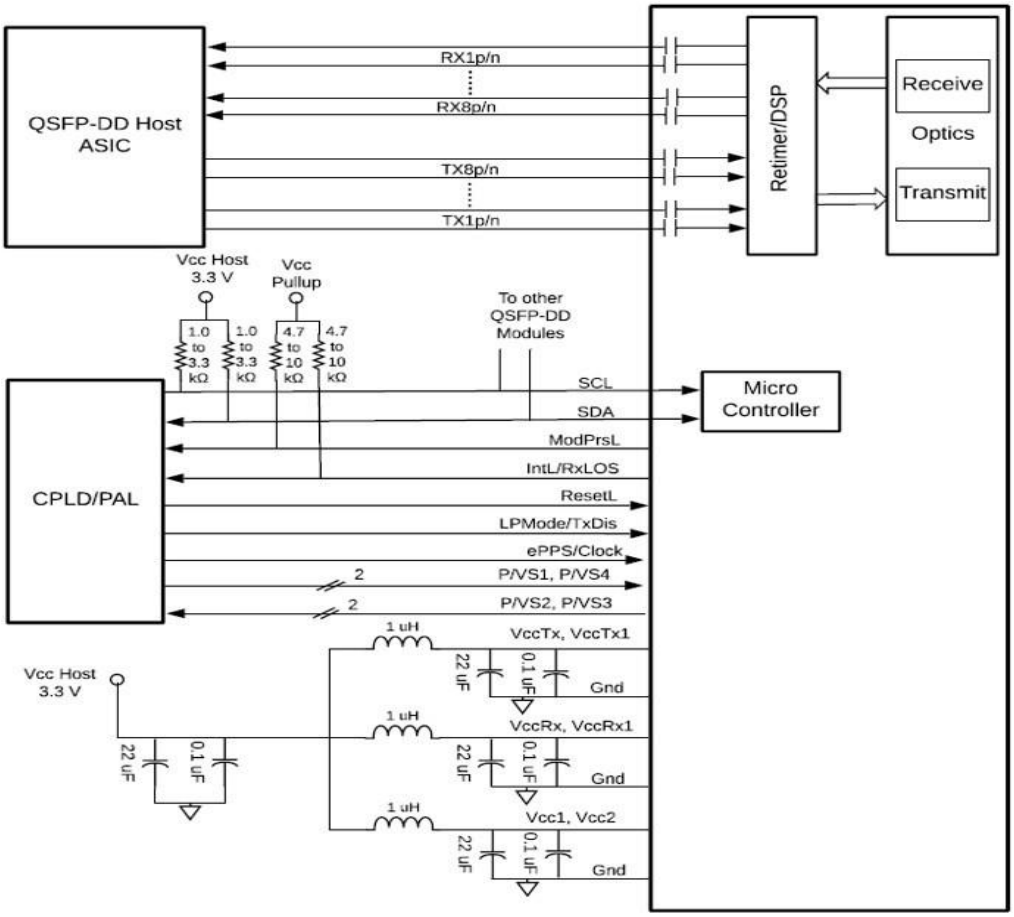
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1B	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	+3.3 V Power Supply Transmitter	2A	2
68		Vcc2	+3.3 V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference		
70		GND	Ground	1A	1

71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

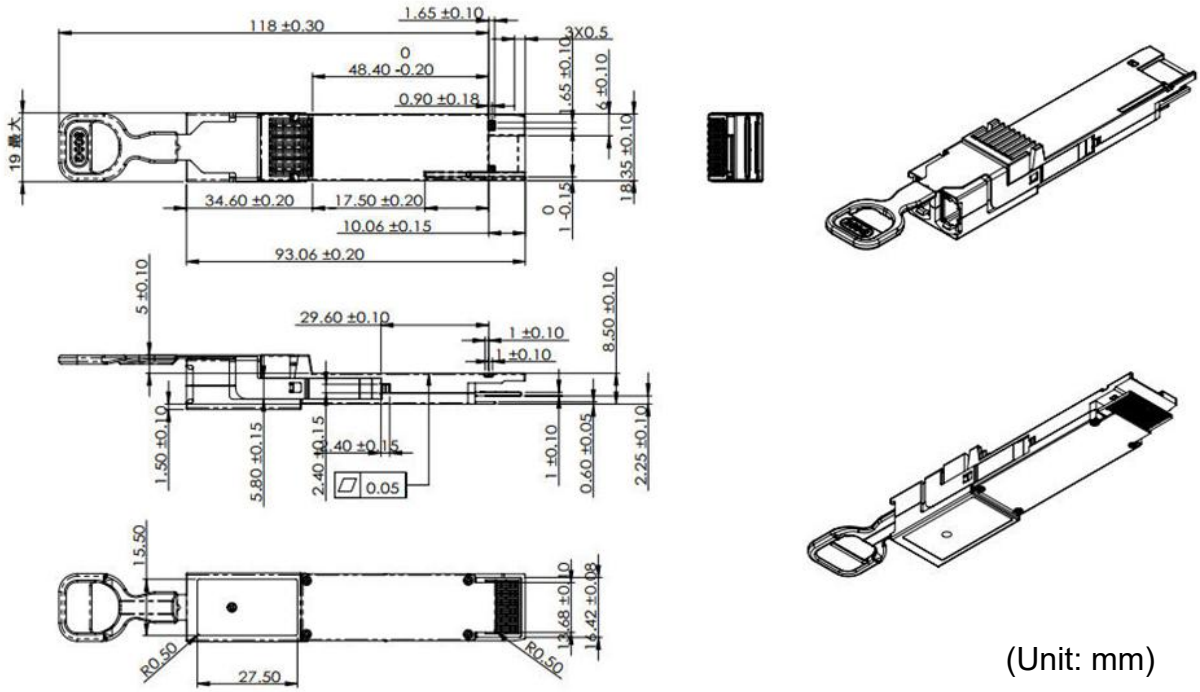
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Recommended block diagram with host board's connections



Package Dimensions



(Unit: mm)

Ordering Information

Part No	Package	Data rate	Reach	Operating Temperature	Application Code	Note
WST-QD8-SR4X2-C	**QSFP-DD**	**106.25 Gb/s (PAM4) per lane**	**100m**	**0 °C to 70 °C**	**800G Ethernet**	**DDM RoHS**

Modification History

Revision	Date	Description	Originator	Review	Approve
V1.0	5-Nov-2025	New Issue	Henry Chung	Wayne Liao	Tom Tang
V1.1	8-Apr-2026	Update typical power consumption and split mode, correct typos	Henry Chung	Wayne Liao	Tom Tang

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