

800G OSFP 2xVR4 Transceiver

P/N: WST-OS8-VR4X2-C



Features:

- OSFP-800 form factor
- 800 Gb/s aggregate data rate
- 8 optical and electrical lanes at 106.25 Gb/s PAM4
- Eight-channel parallel VCSEL transmitters and PIN photodiode receivers with TIAs
- Dual MPO-12/APC optical connector
- 2xVR4 (50 m) optical interface over OM4 multi-mode fiber with host-side KP4 FEC
- Hot pluggable
- Single 3.3 V power supply
- Power consumption: Typical 13 W, Max. 15 W
- Operating case temperature: 0 °C to +70 °C
- Digital diagnostic monitoring support

Applications:

- 800 Gigabit Ethernet or InfiniBand links over multimode fiber
- Data center interconnect applications
- Switch-to-switch and switch-to-router interconnections

Standards:

- IEEE 802.3db and IEEE 802.3ck compliant
- OSFP MSA compliant
- CMIS management interface compliant with CMIS 5.2
- RoHS compliant

Description

The WST-OS8-VR4X2-C module is an 800Gb/s OSFP-800 optical transceiver designed for short-reach multimode fiber (MMF) transmission. It provides eight electrical lanes operating at 106.25 Gb/s PAM4 signaling and supports a 2xVR4 optical interface for transmission distances up to 50 m over OM4 multimode fiber.

The module integrates optical and electrical components within an OSFP-800 form factor and uses dual MPO-12/APC connectors for optical connectivity. The optical transmitters are based on 850 nm VCSEL technology and the receivers use PIN photodiodes, optimized for short-reach multimode fiber applications.

Functional Description

The WST-OS8-VR4X2-C module converts 8 x 106.25 Gb/s PAM4 electrical input signals into optical outputs through integrated transmit circuitry and VCSEL laser drivers, enabling 800 Gigabit Ethernet links over multimode fiber. The optical interface consists of 8 optical lanes using dual MPO-12/APC connectors. On the receive side, incoming optical signals are converted into electrical signals through PIN photodetectors and receiver circuitry. The module is designed for operation in systems employing host-side KP4 forward error correction (FEC) to meet link performance requirements. The module supports digital diagnostic monitoring (DDM) through the OSFP management interface, enabling monitoring of key operating parameters.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	TS	-40	85	°C	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity	RH	5	85	%	
Receiver Damage Threshold (per lane)			+5	dBm	1

Note 1: This parameter defines the maximum optical input power the receiver can withstand without damage and is not an operating condition.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Electrical Signal Rate (per lane)		53.125 ± 100 ppm			GBd	
Optical Signal Rate (per lane)		53.125 ± 100 ppm			GBd	
Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Operating Case Temperature	T _C	0		70	°C	
Power Consumption	P _C		13	15	W	
Supply Current	I _{CC}		3940	4784	mA	
Pre-FEC Bit Error Ratio				2.4 x 10 ⁻⁴		
Post-FEC Bit Error Ratio				1 x 10 ⁻¹²		1
Link Distance (OM4)	DI	0.5		50	m	2

Notes:

1. KP4 FEC provided by host system.
2. KP4 FEC required on host system to support maximum distance.

Optical Characteristics (Under Recommended Operating Conditions)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Signaling speed (per lane)			53.125 ± 100 ppm		GBd	

Modulation format		PAM4				
Lane wavelengths	λ	840		948	nm	
RMS spectral width				0.65	nm	1
Average launch power (per lane)	P	-4.6		4	dBm	2
OMA _{outer} (per lane)	P _{OMA}				dBm	2, 3
For max (TECQ, TDECQ) \leq 1.8 dB		-2.6		3.5		
For 1.8 < max (TECQ, TDECQ) \leq 4.4 dB		-4.4 + max (TECQ, TDECQ)		3.5		
Transmitter and dispersion eye closure for PAM4 (TDECQ) (per lane)				4.4	dB	
Transmitter eye closure for PAM4 (TECQ) (per lane)				4.4	dB	
Extinction ratio (per lane)	ER	2.5			dB	
Average launch power of OFF transmitter (per lane)	P _{off}			-30	dBm	
RIN _{21OMA}	RIN			-132	dB/Hz	
Optical return loss tolerance				14	dB	
Encircled flux		\geq 86 % at 19 μ m \leq 30 % at 4.5 μ m				4
Receiver						
Signaling speed (per lane)		53.125 \pm 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths	λ	840		948	nm	
Average receive power (per lane)		-6.3		4	dBm	5
Receive power (OMA _{outer}) (per lane)	R _{OMA}			3.5	dBm	
Receiver Reflectance				-15	dB	
Receiver sensitivity (OMA _{outer}) (per lane)	SEN	Max(-4.4, -6.2 + TECQ)			dBm	6
Conditions of stressed receiver sensitivity test:						7
Stressed eye closure for PAM4 (SECQ), lane under test		4.4			dB	
OMA _{outer} of each aggressor lane		3.5			dBm	
LOS Assert		-15			dBm	
LOS De-Assert				-6.6	dBm	
LOS Hysteresis		0.5			dB	

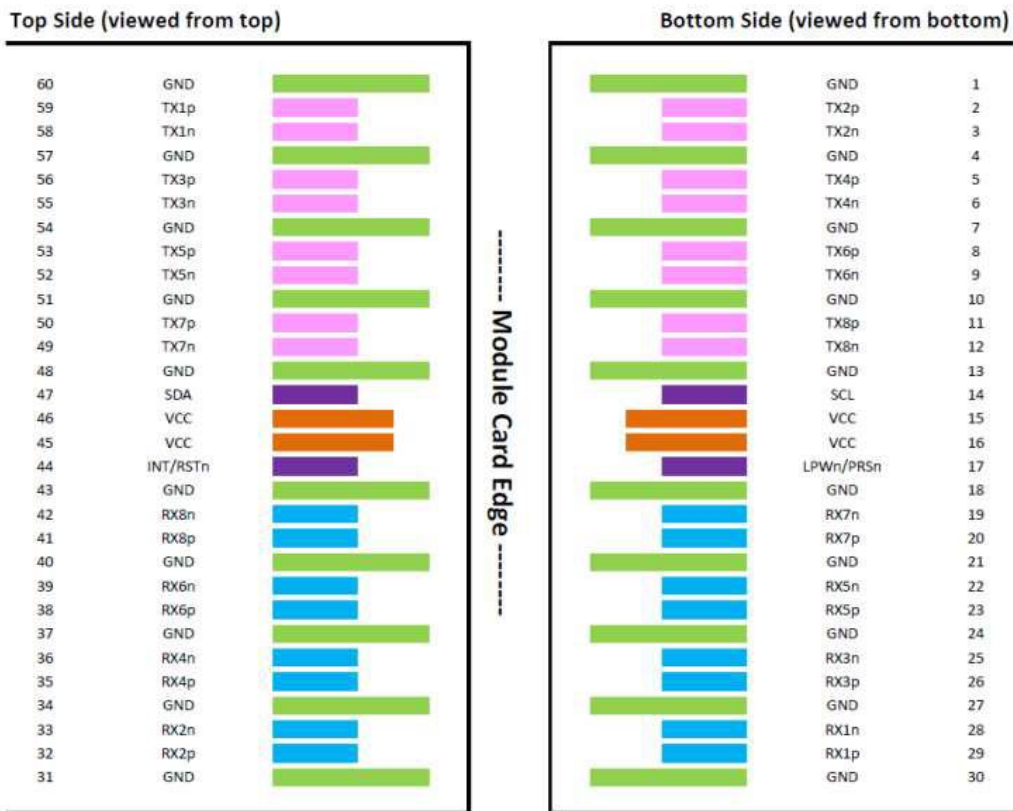
Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Based on stressed receiver sensitivity of -2 dBm, and may increase by up to 0.4 dB based on the choice of stressed receiver sensitivity.
3. Even if the TDECQ < 1.4 dB, the OMA (min) must exceed this value.
4. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μ m fiber, in accordance with IEC 61280-1-4.
5. Average receive power, per lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ up to 4.4 dB.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Monitoring Functions (Under Recommended Operating Conditions)

Parameter	Accuracy	Unit	Note
Measured transceiver case temperature	±3	°C	
Measured transceiver supply voltage	±3	%	
Measured Tx bias current	±10	%	
Measured Tx output power	±3	dB	
Measured Rx received average optical power	±3	dB	

Pin Assignment



Pin out of Connector Block on Host Board

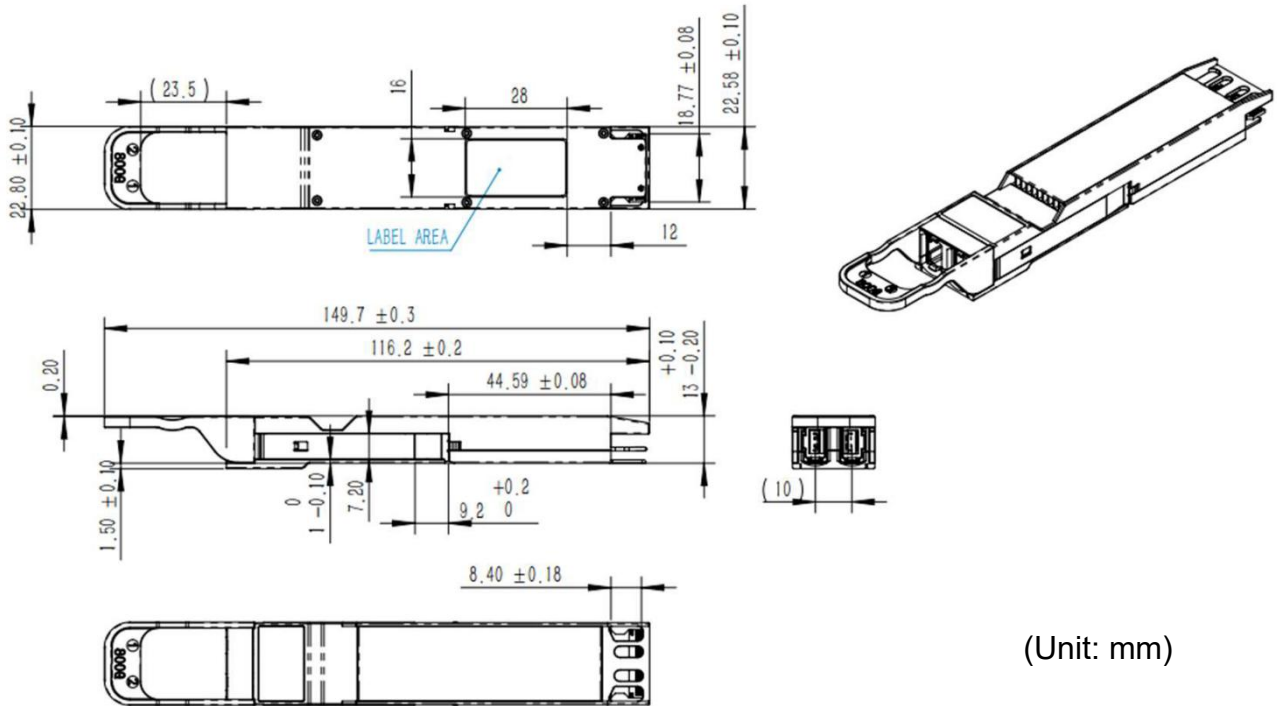
Name	Direction	Description
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receive differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in the OSFP Specification.

INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in OSFP Specification.
VCC	power	3.3V power for module.
GND	ground	Module Ground. Logic and power return path.

Pin	Name	Logic	Description	Notes
1	GND		Ground	
2	TX2p	CML-I	Transmitter Data Non-Inverted	
3	TX2n	CML-I	Transmitter Data Inverted	
4	GND		Ground	
5	TX4p	CML-I	Transmitter Data Non-Inverted	
6	TX4n	CML-I	Transmitter Data Inverted	
7	GND		Ground	
8	TX6p	CML-I	Transmitter Data Non-Inverted	
9	TX6n	CML-I	Transmitter Data Inverted	
10	GND		Ground	
11	TX8p	CML-I	Transmitter Data Non-Inverted	
12	TX8n	CML-I	Transmitter Data Inverted	
13	GND		Ground	
14	SCL	LVC MOS-I/O	2-wire Serial interface clock	
15	VCC		+3.3V Power	
16	VCC		+3.3V Power	
17	LPWn/PRSn	Multi-Level	Low-Power Mode / Module Present	
18	GND		Ground	
19	RX7n	CML-O	Receiver Data Inverted	
20	RX7p	CML-O	Receiver Data Non-Inverted	
21	GND		Ground	
22	RX5n	CML-O	Receiver Data Inverted	
23	RX5p	CML-O	Receiver Data Non-Inverted	
24	GND		Ground	
25	RX3n	CML-O	Receiver Data Inverted	
26	RX3p	CML-O	Receiver Data Non-Inverted	
27	GND		Ground	
28	RX1n	CML-O	Receiver Data Inverted	
29	RX1p		Receiver Data Non-Inverted	
30	GND		Ground	

31	GND		Ground	
32	RX2p	CML-O	Receiver Data Non-Inverted	
33	RX2n	CML-O	Receiver Data Inverted	
34	GND		Ground	
35	RX4p	CML-O	Receiver Data Non-Inverted	
36	RX4n	CML-O	Receiver Data Inverted	
37	GND		Ground	
38	RX6p	CML-O	Receiver Data Non-Inverted	
39	RX6n	CML-O	Receiver Data Inverted	
40	GND		Ground	
41	RX8p	CML-O	Receiver Data Non-Inverted	
42	RX8n	CML-O	Receiver Data Inverted	
43	GND		Ground	
44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	
45	VCC		+3.3V Power	
46	VCC		+3.3V Power	
47	SDA	LVC MOS-I/O	2-wire Serial interface data	
48	GND		Ground	
49	TX7n	CML-I	Transmitter Data Inverted	
50	TX7p	CML-I	Transmitter Data Non-Inverted	
51	GND		Ground	
52	TX5n	CML-I	Transmitter Data Inverted	
53	TX5p	CML-I	Transmitter Data Non-Inverted	
54	GND		Ground	
55	TX3n	CML-I	Transmitter Data Inverted	
56	TX3p	CML-I	Transmitter Data Non-Inverted	
57	GND		Ground	
58	TX1n	CML-I	Transmitter Data Inverted	
59	TX1p	CML-I	Transmitter Data Non-Inverted	
60	GND		Ground	

Package Dimensions



(Unit: mm)

Ordering Information

Part No	Package	Data rate	Reach	Operating Temperature	Application Code	Note
WST-OS8-VR4X2-C	OSFP	106.25 Gb/s (PAM4) per lane	50 m	0 °C to 70 °C	800G Ethernet	DDM RoHS

Modification History

Revision	Date	Description	Originator	Review	Approve
V1.0	21-Feb-2024	New Issue	Henry Chung	Wayne Liao	Tom Tang



Headquarters

6 F., No. 57, Nanxing Rd., Xizhi Dist., New Taipei City 221026, Taiwan
 Tel: +886-2-2698-7208
 Fax: +886-2-2698-7210
 Email: sales@wavesplitter.com
 Website: https://wavesplitter.com