Data Sheet

800G OSFP 2xDR4 Transceiver Module
P/N: WST-OS8-DR4X2-C

Features:

- OSFP form factor
- Supports a single 800 Gb/s aggregate data rate
- 8 optical and electrical lanes at 106.25 Gb/s PAM4
- 8 duplex transmit and receive lanes
- Dual MPO-12/APC optical connector
- 2xDR4 (500 m) optical interface over single-mode fiber with host-side FEC
- Digital diagnostic monitoring support
- Single 3.3 V power supply
- Power consumption: Typical 11.5 W, Max. 15 W
- Operating case temperature: 0 °C to +70 °C

Applications:

- 800 Gigabit Ethernet links over single-mode fiber
- Supports 2 x 400 G, 4 x 200 G, and 8 x 100 G split modes for breakout applications, with partial link capability
- Data center interconnect
- Switch-to-switch and switch-to-router interconnections

Standards:

- IEEE 802.3cn and IEEE 802.3ck compliant
- OSFP MSA compliant
- CMIS management interface compliant with CMIS 5.2 or later
- RoHS compliant

Description

The WST-OS8-DR4X2-C module is an 800G optical transceiver designed for single-mode fiber (SMF) transmission. It provides eight electrical lanes operating at 106.25 Gb/s PAM4 signaling and supports a 2xDR4 optical interface for transmission distances up to 500 m over SMF. The module is implemented in an OSFP form factor and utilizes an MPO-12/APC connector for optical connectivity.

The optical engine is based on silicon photonics (SiPh) technology, incorporating a PIC (photonic integrated circuit) to perform high-speed optical modulation and signal routing. External laser sources are coupled into the SiPh PIC, while photodetectors are implemented using discrete components for optical signal detection. A multi-lane architecture is employed to enable high-density integration and efficient high-speed optical transmission. The module integrates a DSP-based electrical interface to support PAM4 signal processing and ensure reliable high-speed data transmission. It is intended for 800G Ethernet and Datacom applications.

Functional Description

The WST-OS8-DR4X2-C module converts 8 × 106.25 Gb/s PAM4 electrical input signals into optical outputs, enabling 800G Ethernet links over single-mode fiber. The optical interface consists of 8 transmit and receive lanes through dual MPO-12/APC connectors.

The module is designed for operation in systems employing KR4 forward error correction (FEC) to ensure reliable data transmission. It supports standard OSFP management interfaces, allowing system-level configuration, status monitoring, and fault reporting. This module is suitable for high-speed data center and interconnect applications requiring high bandwidth and reliable short-reach optical links.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity	RH	5	85	%	Non-condensing
Receiver Damage Threshold (per lane)	R_D		+5	dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Electrical Signal Rate (per lane)		53.125 ± 100 ppm			GBd	
Optical Signal Rate (per lane)		53.125 ± 100 ppm			GBd	
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Operating Case Temperature	T_C	0		70	°C	
Power Consumption	P_C		11.5	15	W	
Supply Current	Icc		3485	4785	mA	
Link Distance (G.652)	DI	2		500	m	

Optical Characteristics (Under Recommended Operating Conditions)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Signaling speed (per lane)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths	λ	1304.5	1310	1317.5	nm	
Average launch power (per lane)	P	-2.9		4	dBm	1
OMAouter (per lane)	P_{OMA}	-0.8		4.2	dBm	2
Launch power in OMAouter minus TDECQ (per lane)		-2.2			dB	
Transmitter and dispersion eye closure for PAM4				3.4	dB	

(TDECQ) (per lane)						
Side mode suppression ratio (SMSR)		30			dB	
Extinction ratio	ER	3.5			dB	
Average launch power of OFF transmitter (per lane)	P_{off}			-15	dBm	
$RIN_{21}OMA$	RIN			-136	dB/Hz	
Optical return loss tolerance				21.4	dB	
Transmitter reflectance				-26		3
Receiver						
Signaling speed (per lane)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths	λ	1304.5	1310	1317.5	nm	
Average receive power (per lane)		-5.9		4	dBm	4
Receive power (OMAouter) (per lane)	R_{OMA}			4.2	dBm	
Receiver Reflectance				-26	dB	
Receiver sensitivity (OMAouter) (per lane)	SEN	max(-3.9, SECQ-5.3)			dBm	5
LOS Assert		-26			dBm	
LOS De-Assert				-8	dBm	
LOS Hysteresis		0.5			dB	

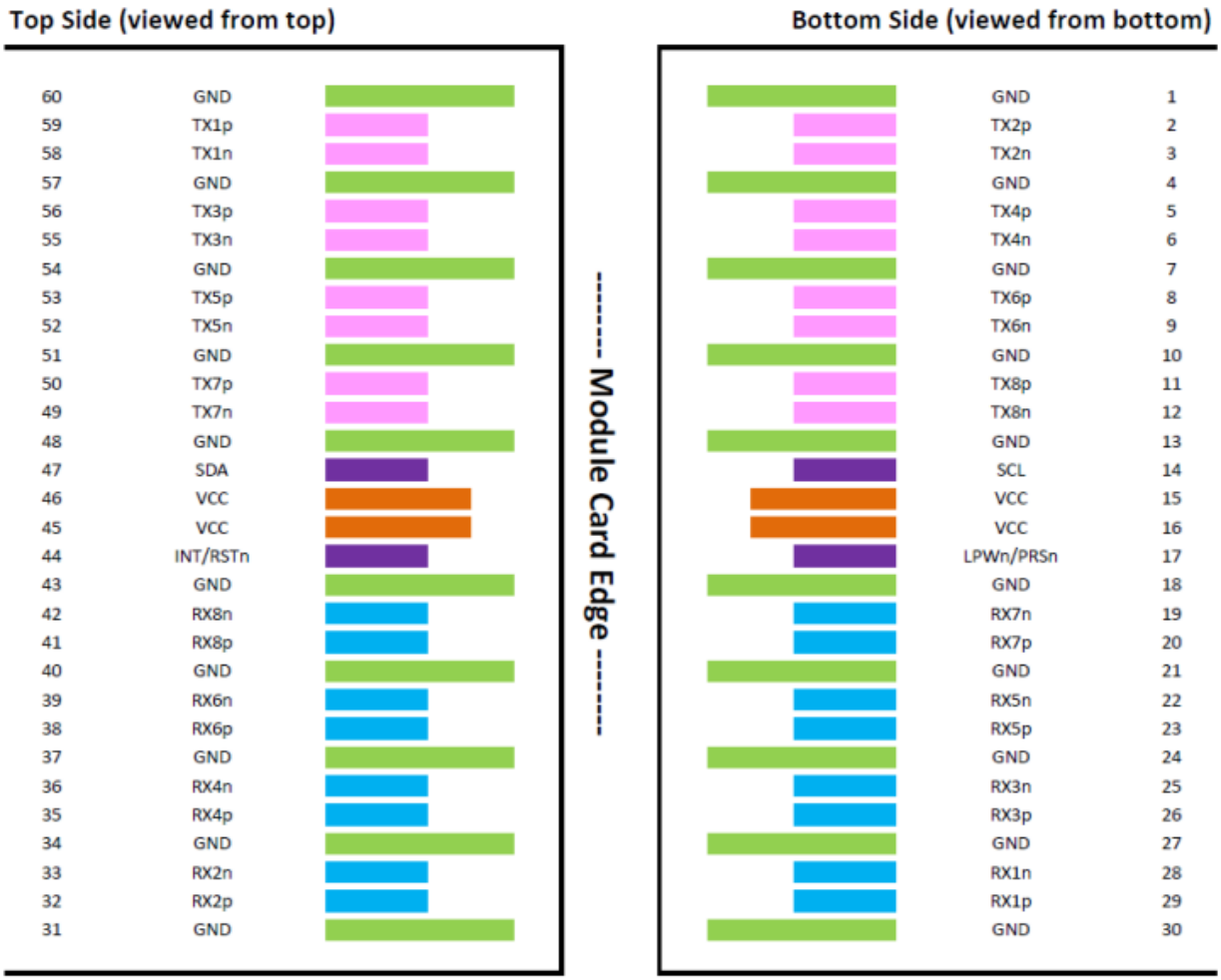
Notes:

1. Average launch power, per lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed these values.
3. Transmitter reflectance is defined looking into the transmitter.
4. Average receive power, per lane(min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMAouter), per lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4dB.

Digital Diagnostic Monitoring Accuracy (Under Recommended Operating Conditions)

Parameter	Accuracy	Unit	Note
Measured transceiver case temperature	±3	°C	
Measured transceiver supply voltage	±3	%	
Measured Tx bias current	±10	%	
Measured Tx output power	±3	dB	
Measured Rx received average optical power	±3	dB	

Pin Assignment



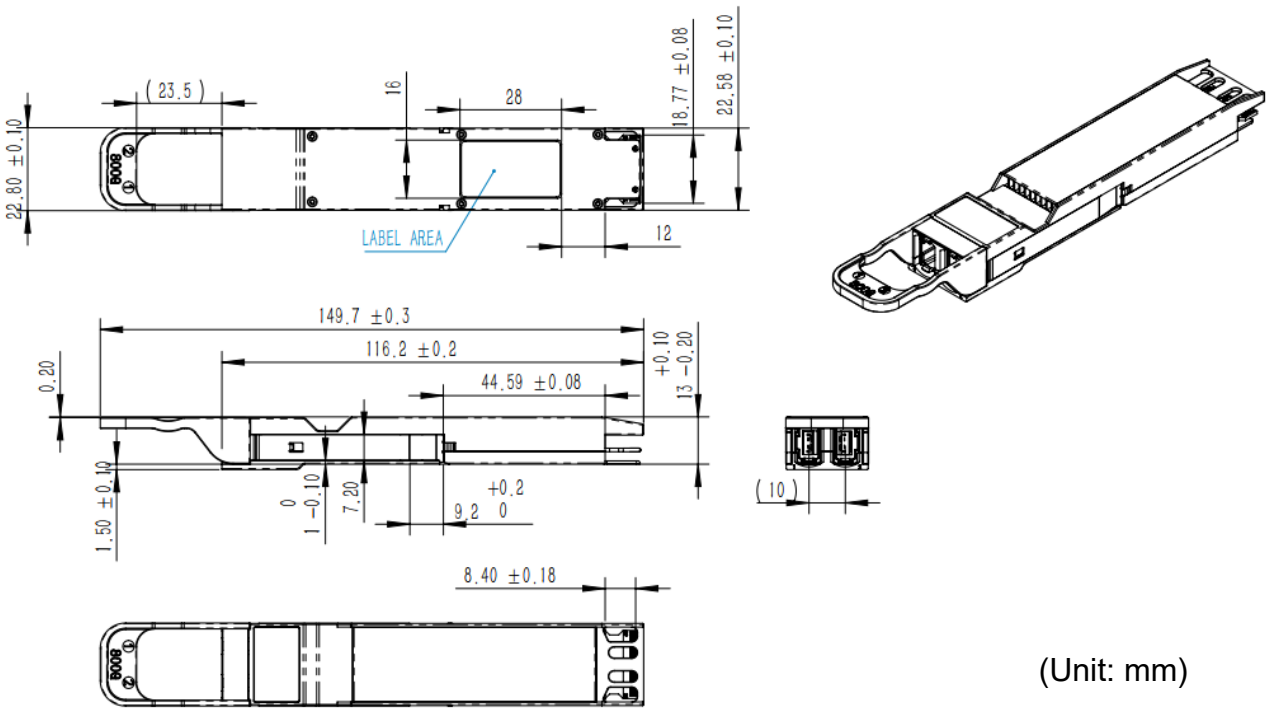
Pin out of Connector Block on Host Board

Name	Direction	Description
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receive differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	bidir	Multi level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in the OSFP Specification.
INT/RSTn	bidir	Multi level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in OSFP Specification.
VCC	power	3.3V power for module.
GND	ground	Module Ground. Logic and power return path.

Pin	Logic	Symbol	Description	Notes
1	GND		Ground	
2	TX2p	CML-I	Transmitter Data Non-Inverted	
3	TX2n	CML-I	Transmitter Data Inverted	
4	GND		Ground	
5	TX4p	CML-I	Transmitter Data Non-Inverted	
6	TX4n	CML-I	Transmitter Data Inverted	
7	GND		Ground	
8	TX6p	CML-I	Transmitter Data Non-Inverted	
9	TX6n	CML-I	Transmitter Data Inverted	
10	GND		Ground	
11	TX8p	CML-I	Transmitter Data Non-Inverted	
12	TX8n	CML-I	Transmitter Data Inverted	
13	GND		Ground	
14	SCL	LVCMOS-I/O	2-wire Serial interface clock	
15	VCC		+3.3V Power	
16	VCC		+3.3V Power	
17	LPWn/PRSn	Multi-Level	Low-Power Mode / Module Present	
18	GND		Ground	
19	RX7n	CML-O	Receiver Data Inverted	
20	RX7p	CML-O	Receiver Data Non-Inverted	
21	GND		Ground	
22	RX5n	CML-O	Receiver Data Inverted	
23	RX5p	CML-O	Receiver Data Non-Inverted	
24	GND		Ground	
25	RX3n	CML-O	Receiver Data Inverted	
26	RX3p	CML-O	Receiver Data Non-Inverted	
27	GND		Ground	
28	RX1n	CML-O	Receiver Data Inverted	
29	RX1p		Receiver Data Non-Inverted	
30	GND		Ground	
31	GND		Ground	
32	RX2p	CML-O	Receiver Data Non-Inverted	
33	RX2n	CML-O	Receiver Data Inverted	
34	GND		Ground	

35	RX4p	CML-O	Receiver Data Non-Inverted	
36	RX4n	CML-O	Receiver Data Inverted	
37	GND		Ground	
38	RX6p	CML-O	Receiver Data Non-Inverted	
39	RX6n	CML-O	Receiver Data Inverted	
40	GND		Ground	
41	RX8p	CML-O	Receiver Data Non-Inverted	
42	RX8n	CML-O	Receiver Data Inverted	
43	GND		Ground	
44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	
45	VCC		+3.3V Power	
46	VCC		+3.3V Power	
47	SDA	LVCMOS-I/O	2-wire Serial interface data	
48	GND		Ground	
49	TX7n	CML-I	Transmitter Data Inverted	
50	TX7p	CML-I	Transmitter Data Non-Inverted	
51	GND		Ground	
52	TX5n	CML-I	Transmitter Data Inverted	
53	TX5p	CML-I	Transmitter Data Non-Inverted	
54	GND		Ground	
55	TX3n	CML-I	Transmitter Data Inverted	
56	TX3p	CML-I	Transmitter Data Non-Inverted	
57	GND		Ground	
58	TX1n	CML-I	Transmitter Data Inverted	
59	TX1p	CML-I	Transmitter Data Non-Inverted	
60	GND		Ground	

Package Dimensions



(Unit: mm)

Ordering Information

Part No	Package	Data rate	Reach	Operating Temperature	Application Code	Note
WST-OS8-DR4X2-C	**OSFP**	**106.25 Gb/s (PAM4) per lane**	**500 m**	**0 °C to 70 °C**	**800G Ethernet**	**DDM RoHS**

Modification History

Revision	Date	Description	Originator	Review	Approve
V1.0	21-Feb-2024	New Issue	Henry Chung	Wayne Liao	Tom Tang

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