DataSheet

800G QSFP-DD Direct Attach Cable

WS-QD8-DACPx-xx

Features:

- Up to 53.125 GBd PAM4 data rate per lane
- 3.3V supply for EEPROM and management interface
- I2C for EEPROM communication, pull to Release latch design
- Excellent EMI/EMC performance with 360 degree cable shield termination
- 28~26 AWG high performance twinax cable
- Low loss, stronger mechanical features, more flexible
- Hot-pluggable
- Operating case temperature: -40 to +85 °C

Applications:

- Data Center & Networking Equipment
- Servers / Storage Devices
- High Performance Computing (HPC)
- Switches / Routers

Standard:

- IEEE 802.3ck 800G electrical interface
- QSFP-DD MSA Mechanical and Pinout
- CMIS Rev. 4.0 Management Interface
- RoHS Compliant

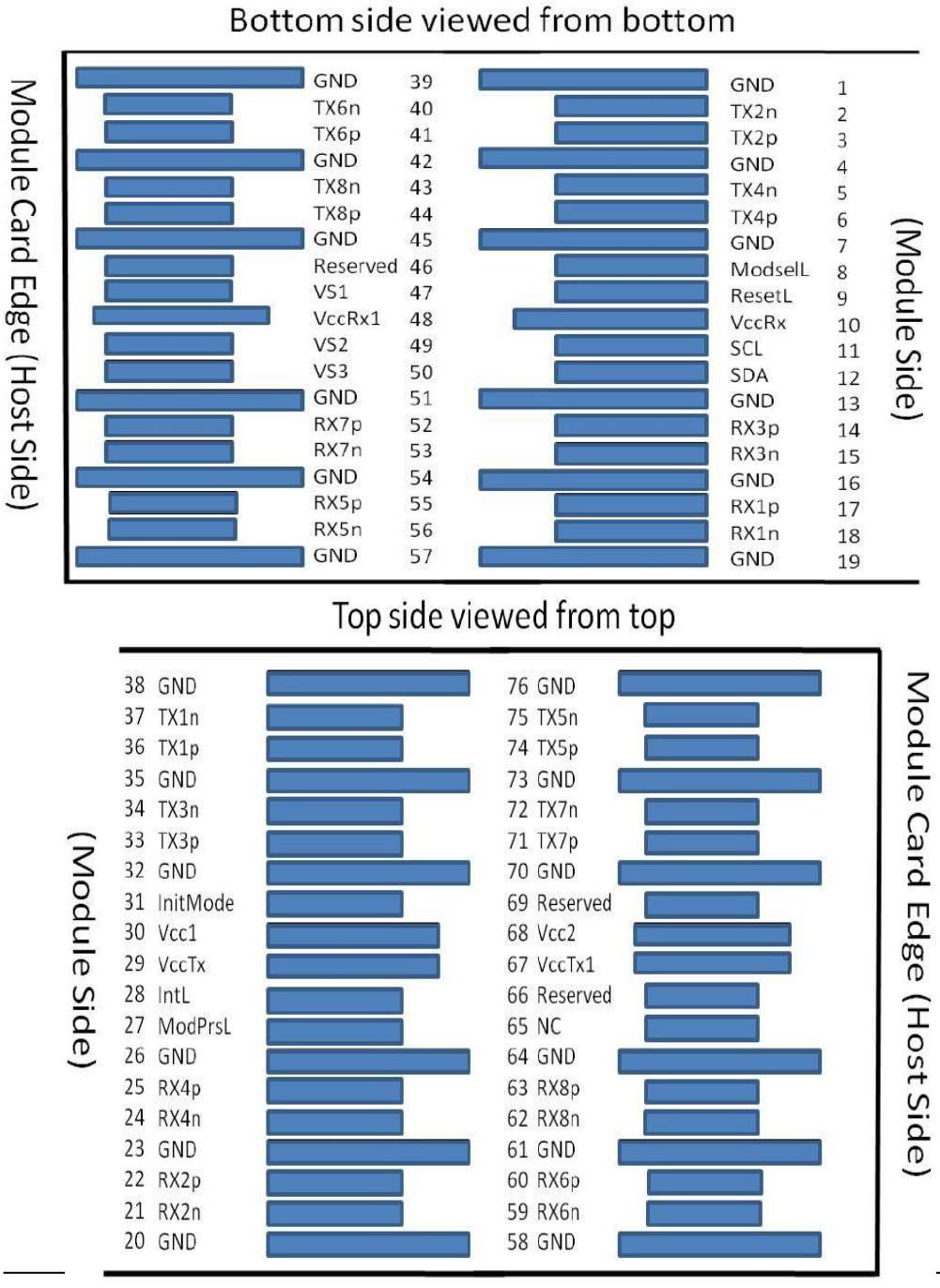
Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	Ts	-40		85	ºC	
Relative Humidity	RH	5		85	%	Non condensation
Power Supply Voltage	V_{CC}	0		3.6	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	T_{case}	-40		85	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate	BR		53.125		GBd	Per lane

QSFP-DD Module Pad Assignments



Pin	Logic	Symbol	Description	Notes
1		GND	Ground	
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	1

33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2

68		Vcc2	3.3V Power Supply	2
69		Reserved	For Future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Note:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

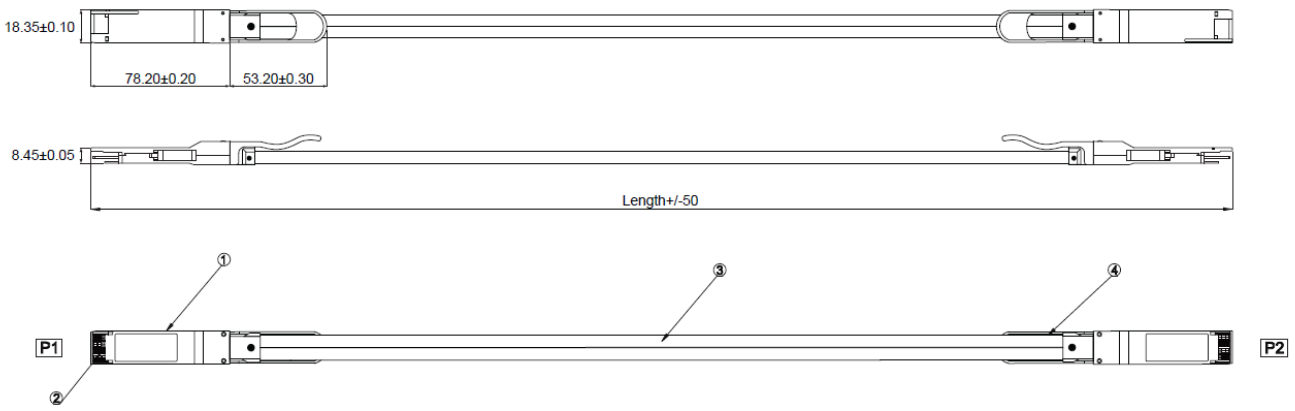
Wiring Diagram

P1 QSFP-DD SIGNAL	PAD	QSFP-DD PAD	SIGNAL P2
GND	1	20	GND
TX2n	2	21	RX2n
TX2p	3	22	RX2p
GND	4	23	GND
TX4n	5	24	RX4n
TX4p	6	25	RX4p
GND	7	26	GND
GND	13	32	GND
RX3p	14	33	TX3p
RX3n	15	34	TX3n
GND	16	35	GND
RX1p	17	36	TX1p
RX1n	18	37	TX1n
GND	19	38	GND
GND	20	1	GND
RX2n	21	2	TX2n
RX2p	22	3	TX2p
GND	23	4	GND
RX4n	24	5	TX4n
RX4p	25	6	TX4p
GND	26	7	GND
GND	32	13	GND
TX3p	33	14	RX3p
TX3n	34	15	RX3n
GND	35	16	GND
TX1p	36	17	RX1p
TX1n	37	18	RX1n
GND	38	19	GND

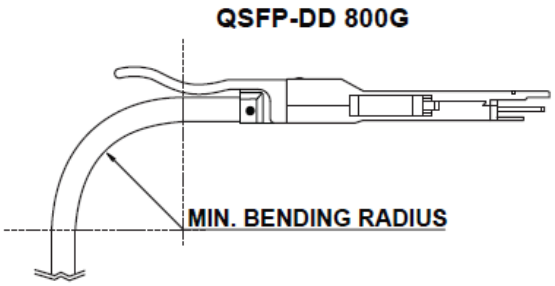
P1 QSFP-DD SIGNAL	PAD	QSFP-DD PAD	SIGNAL P2
GND	39	58	GND
TX6n	40	59	RX6n
TX6p	41	60	RX6p
GND	42	61	GND
TX8n	43	62	RX8n
TX8p	44	63	RX8p
GND	45	64	GND
GND	51	70	GND
RX7p	52	71	TX7p
RX7n	53	72	TX7n
GND	54	73	GND
RX5p	55	74	TX5p
RX5n	56	75	TX5n
GND	57	76	GND
GND	58	39	GND
RX6n	59	40	TX6n
RX6p	60	41	TX6p
GND	61	42	GND
RX8n	62	43	TX8n
RX8p	63	44	TX8p
GND	64	45	GND
GND	70	51	GND
TX7p	71	52	RX7p
TX7n	72	53	RX7n
GND	73	54	GND
TX5p	74	55	RX5p
TX5n	75	56	RX5n
GND	76	57	GND

LOW SPEED SIGNALS P1 & P2	
SIGNAL	PAD
MODSELL	8
RESETL	9
VCCRX	10
SCL	11
SDA	12
MODPRSL	27
INTL	28
VCCTX	29
VCC1	30
INIT_MODE	31
OPEN	46
	47
	48
	49
	50
	65
	66
	67
	68
	69

Mechanical Design Diagram



Bending Radius:



Min. bending radius allowed	Repeated	Single
	10 x ϕ	5 x ϕ

Ordering Information

Part No	Specification				
	Package	Data rate per Lane	Temp.	Gauge	Length
WS-QD8-DACP8-0H	QSFP-DD to QSFP-DD	53.125 GBd PAM4	-40~85 °C	28 AWG	0.5 m ± 0.05 m
WS-QD8-DACP8-1	QSFP-DD to QSFP-DD	53.125 GBd PAM4	-40~85 °C	28 AWG	1.0 m ± 0.05 m
WS-QD8-DACP8-1H	QSFP-DD to QSFP-DD	53.125 GBd PAM4	-40~85 °C	28 AWG	1.5 m ± 0.05 m
WS-QD8-DACP6-2	QSFP-DD to QSFP-DD	53.125 GBd PAM4	-40~85 °C	26 AWG	2.0 m ± 0.08 m

Modification History

Revision	Date	Description	Originator	Reviewed by	Approved by
V1.0	15-Oct-2022	New Issue	Ken Chang	Wayne Liao	Tom Tang

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