Data Sheet

800G QSFP-DD Active Optical Cable

P/N: WS-QD8-AOCxCyyz

Features:

- QSFP-DD Serial Optical Interface
- 8x100G PAM4 retimed 800GAUI-8 electrical interface
- Active Optical Cable
- 8 channel VCSEL arrays and 8 channels PIN photo detector arrays
- Maximum link length of 60m on OM3 or 100m on OM4
- Hot Pluggable QSFP-DD form factor
- Power dissipation < 14W per cable end
- Operating case temp Commercial: 0°C to +70 °C

Applications:

- 800GBASE-AOC 800G Ethernet
- Data center

Standards:

- Compliant to QSFP-DD-Hardware-Rev 6.3 MSA
- Compliant with CMIS 5.2
- Compliant with IEEE 802.3db
- Compliant to IEEE 802.3ck

General Description

The WS-QD8-AOCXCxx3 is a QSFP-DD to QSFP-DD active optical cable for short-range data communication and interconnect applications. Each AOC has 8 duplex channels with 850Gbit/s aggregate bandwidth. Each channel operates with PAM4 modulation scheme at 53.125G baud rate, and up to 60m using OM3 fiber or 100m using OM4 fiber.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit.
Storage Temperature	Ts	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Relative Humidity (non-condensation)	RH	15	85	%
Supply Voltage	Vcc	-0.5	3.6	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit.
Operating Case Temperature	Top	0	70	°C
Relative Humidity (non-condensation)	RH	15	85	%
Power Supply Voltage	Vcc	3.135	3.465	V
Total Power Consumption per end1	Pc		14	W
Supply Current per end			4.46	A
Bit Rate	BR		850	Gbps
I2C Clock Frequency	0		400	kHz

Notes:

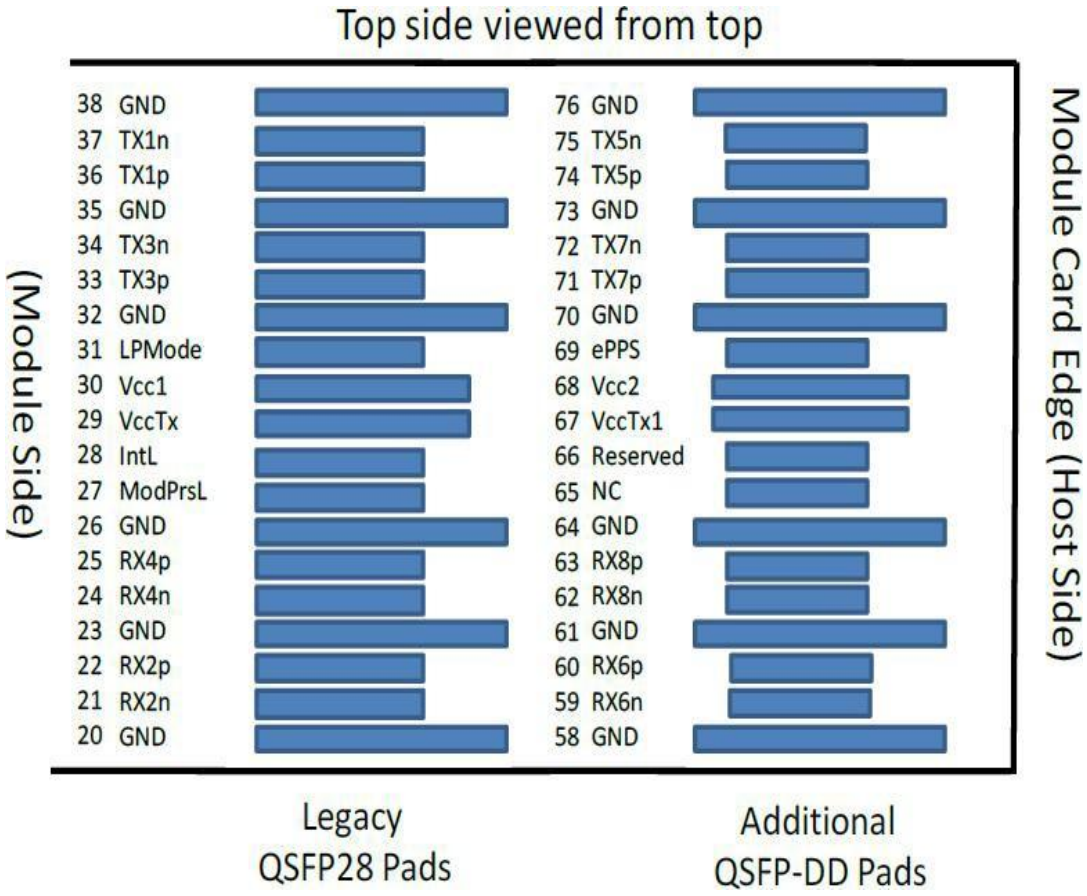
1 Under condition of 3.465V operating supply voltage, and 70℃ case temperature.

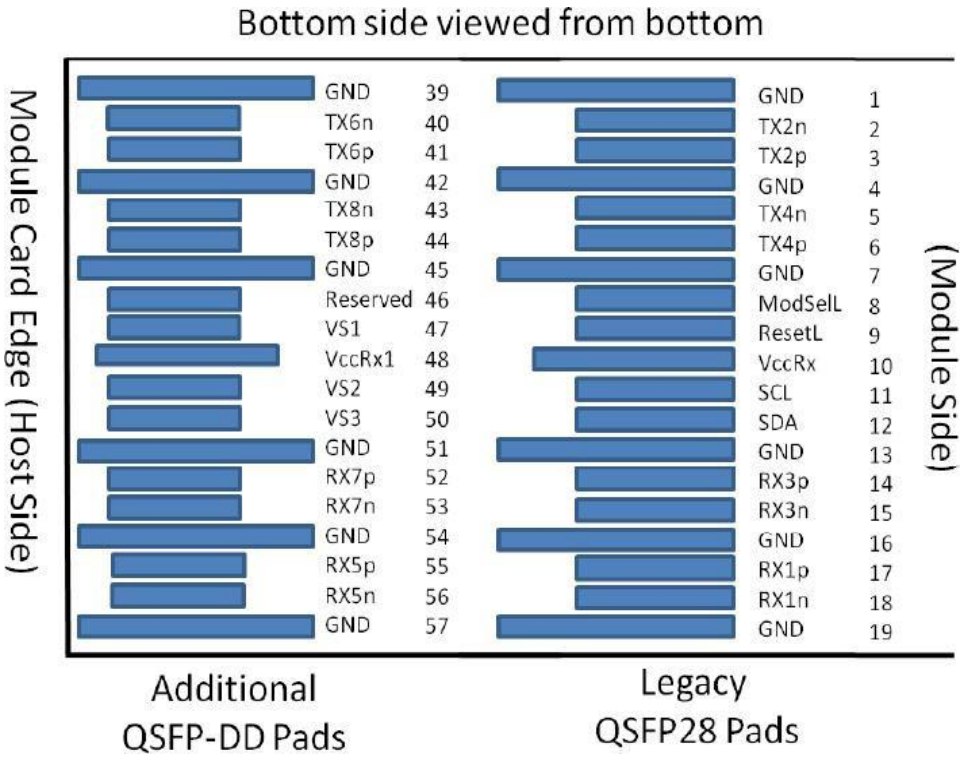
Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit.
Pre FEC Bit Error Ratio			2.4E-4	
Post FEC Bit Error Ratio			1E-12	
Transmitter (each Lane)				
Differential pk-pk Input Voltage tolerance	750			mV
Differential Termination Mismatch			10	%
Eye height	10			mV
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)			dB
Vertical eye closure			12	dB
Effective return loss	7.3			dB

Transition Time	10			ps
Receiver (each Lane)				
Differential data output swing	300		900	mVpp
Differential termination mismatch			10	%
Eye height	15			mV
Vertical eye closure			12	dB
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)			
Effective return loss	8.5			dB
Transition time	8.5			ps

Pin Assignment





PIN	Name	Logic	Description	Power Sequence	Notes
1	Ground		GND	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSelL	LVTTL-I	Module Select	3B	
9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVCMOS-I/O	2-wire serial interface clock	3B	
12	SDA	LVCMOS-I/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1

14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output	3B	
16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1
20	Ground		GND	1B	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3B	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3B	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3B	
26	Ground		GND	1B	1
27	ModPrsL	LVTTL-O	Module Present	3B	
28	IntL	LVTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMode	LVTTL-I	Low Power mode	3B	
32	Ground		GND	1B	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1
39	Ground		GND	1A	1
40	Tx6n	CML-I	Transmitter Inverted Data Input	3A	
41	Tx6p	CML-I	Transmitter Non-Inverted Data Output	3A	
42	Ground		GND	1A	1

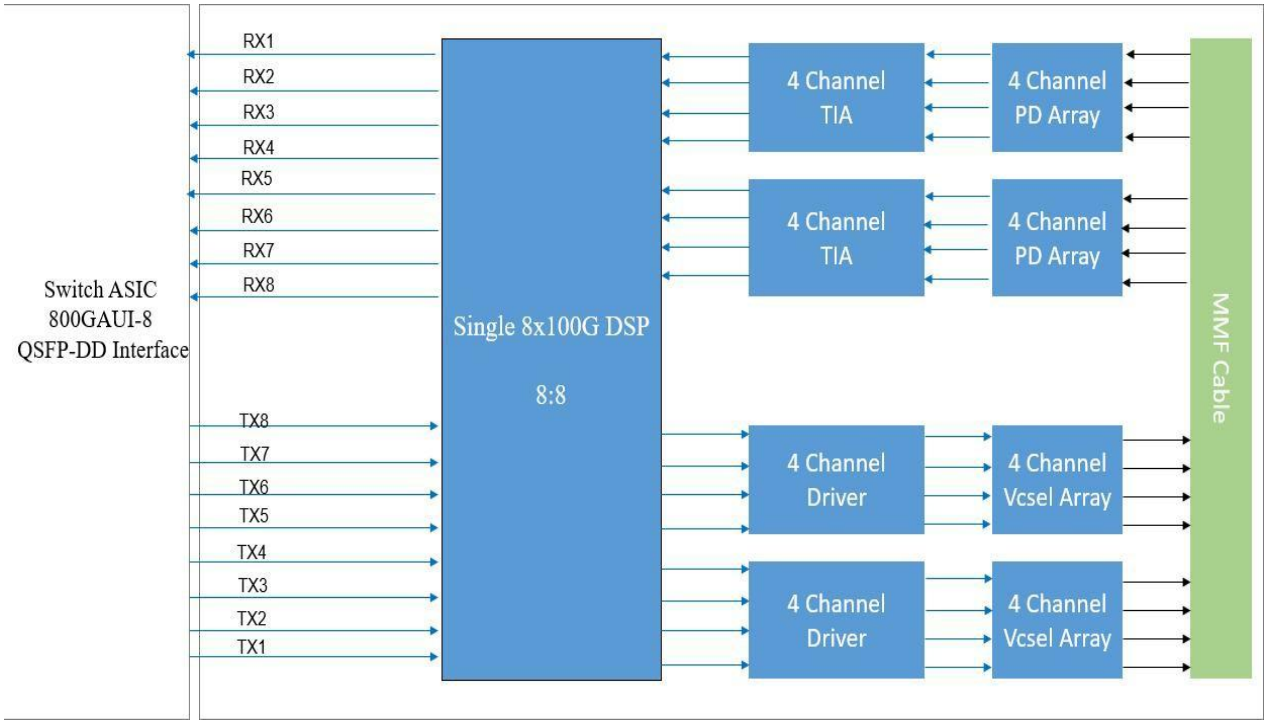
43	Tx8n	CML-I	Transmitter Inverted Data Input	3A	
44	Tx8p	CML-I	Transmitter Non-Inverted Data Output	3A	
45	Ground		GND	1A	1
46	Reserved		For future use	3A	3
47	VS1		Module Vendor Specific1	3A	3
48	VccRx1		3.3V Power Supply	2A	2
49	VS2		Module Vendor Specific2	3A	3
50	VS3		Module Vendor Specific3	3A	3
51	Ground		GND	1A	1
52	Rx7p	CML-O	Receiver Non-Inverted Data Output	3A	
53	Rx7n	CML-O	Receiver Inverted Data Output	3A	
54	Ground		GND	1A	1
55	Rx5p	CML-O	Receiver Non-Inverted Data Output	3A	
56	Rx5n	CML-O	Receiver Inverted Data Output	3A	
57	Ground		GND	1A	1
58	Ground		GND	1A	1
59	Rx6n	CML-O	Receiver Inverted Data Output	3A	
60	Rx6p	CML-O	Receiver Non-Inverted Data Output	3A	
61	Ground		GND	1A	1
62	Rx8n	CML-O	Receiver Inverted Data Output	3A	
63	Rx8p	CML-O	Receiver Non-Inverted Data Output	3A	
64	Ground		GND	1A	1
65	NC		No Connect	3A	3
66	Reseved		For future use	3A	3
67	VccTx1		3.3V Power Supply	2A	2
68	Vcc2		3.3V Power Supply	2A	2
69	ePPS	LVTTL-I	Precision Time Protocol (PTP) reference clock input	3A	3
70	Ground		GND	1A	1
71	Tx7p	CML-I	Transmitter Non-Inverted Data Output	3A	

72	Tx7n	CML-I	Transmitter Inverted Data Output	3A	
73	Ground		GND	1A	1
74	Tx5p	CML-I	Transmitter Non-Inverted Data Output	3A	
75	Tx5n	CML-I	Transmitter Inverted Data Output	3A	
76	Ground		GND	1A	1

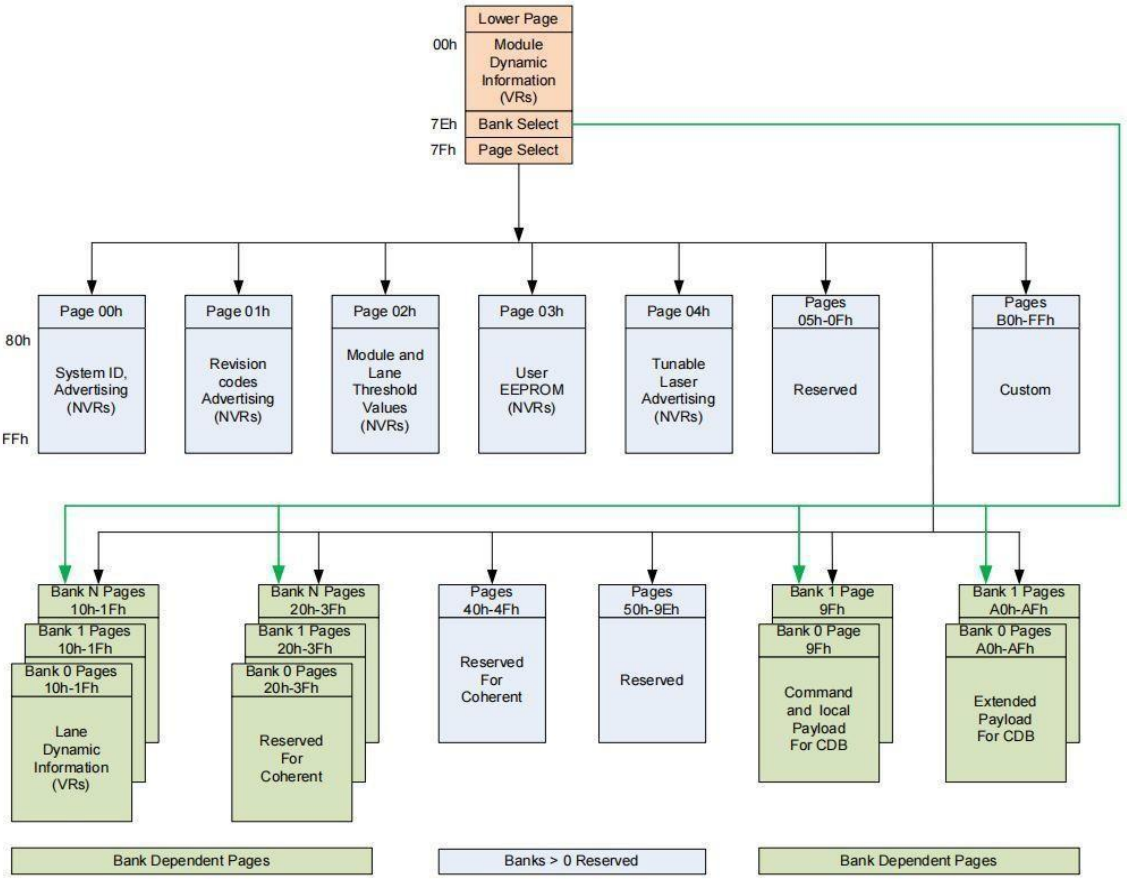
Notes:

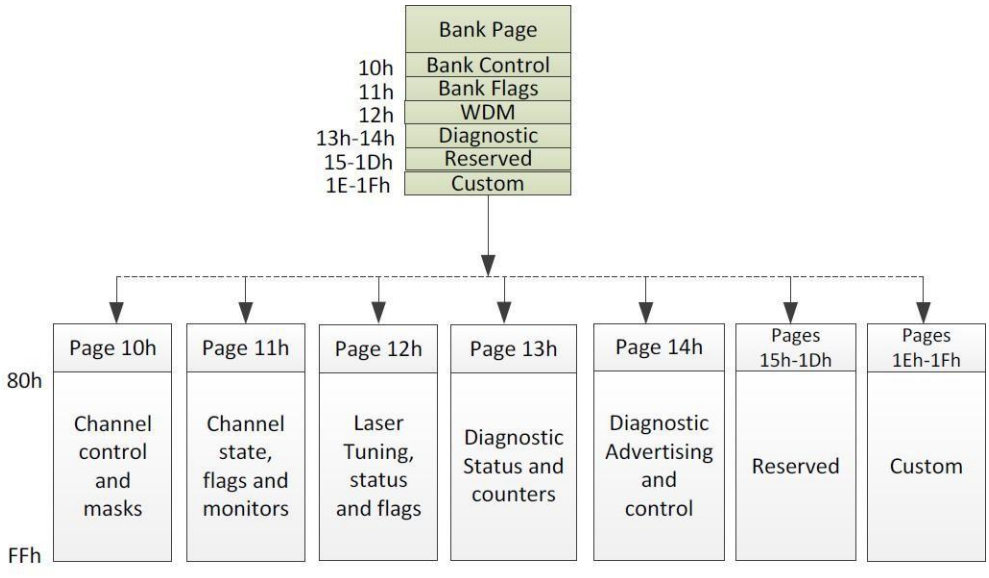
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10Kohms and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, the break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Functional Block Diagram



MEMORY MAP





Multiple Applications Support

The WS-QD8-AOCXCxx3 supports CMIS 5.2 defined Application Advertising, Application Selectionand Instantiation.

Application Selection and Instantiation

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.

*Note that both sides of AOC need to be set to the same application.

WS-QD8-AOCXCxx3 supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized, which is simpler.

First method:

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation. The Active Set can be read from page11h.

For example, select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145~Byte152(8 bytes)—Set AppselCode3

Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

Second method:

Set the value of Page10h Byte240. This is a private definition.

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	100GAUI-1-S C2M	AOC
1	00000001b	400GAUI-8	AOC
2	00000010b	200GAUI-8	AOC
3	00000011b	800G S C2M	AOC

TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

TX input equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

RX output Equalization

RX output Equalization follows CMIS Table, with default 1dB, readable and writable.

Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	**Reserved**	**Reserved**
11-15	1011b-1111b	Custom	Custom

RX output amplitude

RX output amplitude follows CMIS Table, Rx output amplitude is the difference peak-to- peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

Loopback capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method

refers to CMIS.

QSFP-DD Rx Output Equalization code table

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

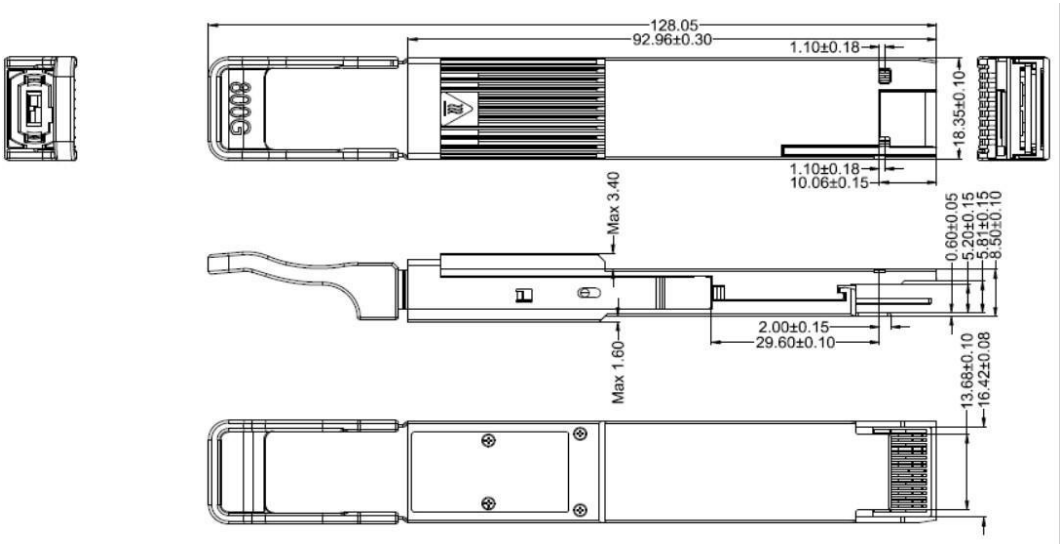
Digital Diagnostic Monitor Accuracy

Parameter	Accuracy	Unit
Internally Measured AOC Temperature1	±3	℃
Internally Measured AOC Supply Voltage	±3	%
Measured Tx Bias Current	±10	%
Measured Tx Output Power2	±3	dB
Measured Rx Received Average Optical Power	±3	dB

Notes:

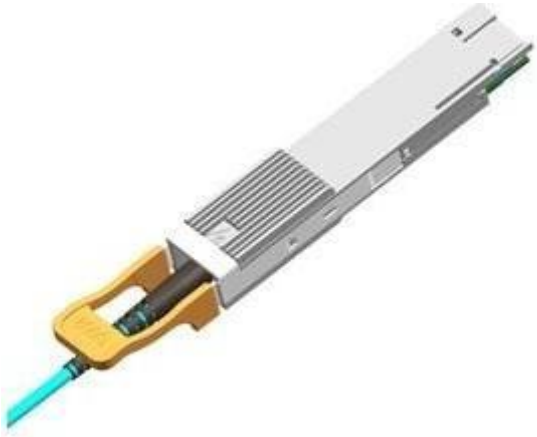
1. Test point is the hotspot of the module.
2. DDM reports stability within 0.5 dB when temperature is stable. TX DDM reportes -40 dBm when TX disable.

Mechanical Drawing



Pull-tab Color

Pull-tab color is Pantone 475U (Beige).



Laser safety

All AOCs are Class 1 Laser products per FDA/CDRH and IEC-60825-1 & IEC60825-2 standards. They must be operated under specified operating conditions.

Electromagnetic Compatibility

All AOCs are designed to meet FCC Class B limits.

Ordering Information

Part No	Specification							
	Package	Data rate	Laser	Fiber	Cable Type	Cable Length	Temp.	Application
WS-QD8-AOCxCyyz	QSFP-DD PAM4	800Gbps	850nm	OM3 or OM4	LSZH, OFNR, OFNP	yy m	0~70°C	800G Ethernet
WS-QD8-AOCXC013	QSFP-DD PAM4	800Gbps	850nm	OM3	LSZH, or OFNR, or OFNP	1 m	0~70°C	800G Ethernet
WS-QD8-AOCXC033	QSFP-DD PAM4	800Gbps	850nm	OM3	LSZH, or OFNR, or OFNP	3 m	0~70°C	800G Ethernet
WS-QD8-AOCXC103	QSFP-DD PAM4	800Gbps	850nm	OM3	LSZH, or OFNR, or OFNP	10 m	0~70°C	800G Ethernet
WS-QD8-AOCXC603	QSFP-DD PAM4	800Gbps	850nm	OM3	LSZH, or OFNR, or OFNP	60 m	0~70°C	800G Ethernet

Note:

Cable type (x): X for LSZH or OFNR or OFNP, L for LSZH, R for OFNR, P for OFNP

Length (yy): two digits in meter

Fiber (z): 3 for OM3, 4 for OM4

Variant Length and Cable Types can be customized. Please contact our sales for detail information.

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	8-Jan-2025	New Issue	Ken Cheng	Tom Tang	Tom Tang
V1.1	13-Jan-2026	Add photo and update ordering info.	Henry Chung	Wayne Liao	Tom Tang

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