

800G OSFP Direct Attach Cable

WS-OS8-DACP_x-xx



Features:

- Up to 53.125 GBd PAM4 data rate per channel
- 3.3V supply for EEPROM and management interface
- I2C for EEPROM communication, pull to Release latch design
- Excellent EMI/EMC performance 360 degree cable shield termination
- 30~26 AWG high performance twinax cable
- Low loss, stronger mechanical features, more flexible
- Hot-pluggable
- -40°C to 85°C case temperature operating range

Applications:

- Data Center & Networking Equipment
- Servers / Storage Devices
- High Performance Computing (HPC)
- Switches / Routers

Standard:

- IEEE 802.3ck 800G electrical interface
- OSFP MSA Rev 5.0 Mechanical and Pinout
- CMIS Rev. 4.0 Management Interface
- RoHS Compliant

Absolute Maximum Ratings

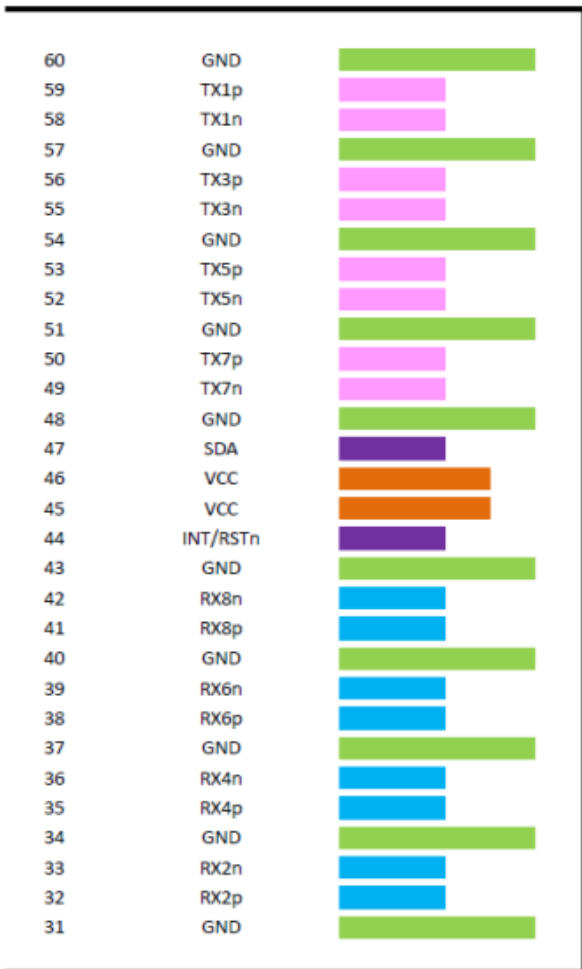
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	T _s	-40		85	°C	
Relative Humidity	RH	5		85	%	Non condensation
Power Supply Voltage	V _{cc}	0		3.6	V	

Recommended Operating Conditions

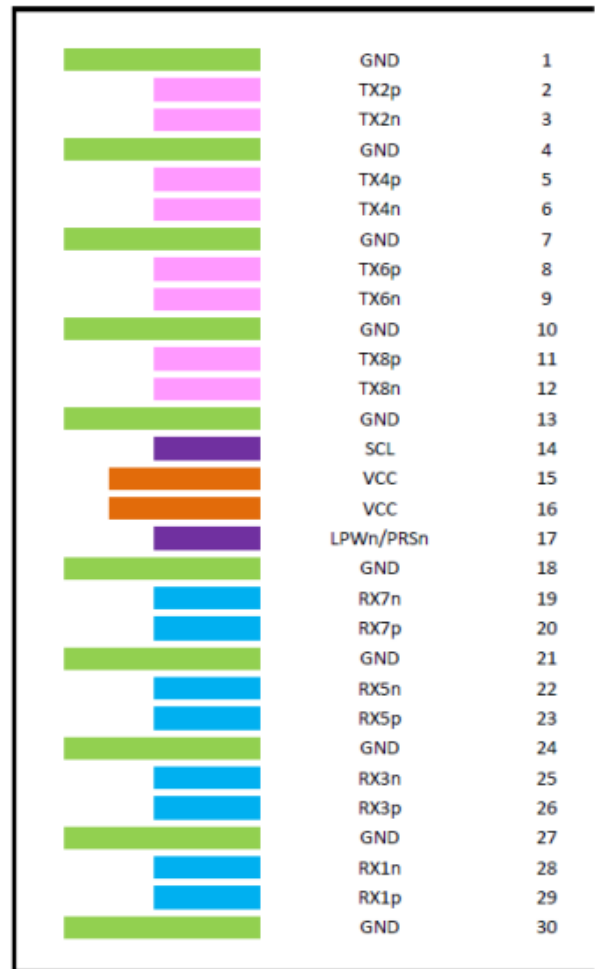
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	T _{case}	-40		85	°C	
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Data Rate	BR		53.125		Gbd	Each channel

MODULE PINOUT (compliant OSFP MSA Rev 5.0)

Top Side (viewed from top)



Bottom Side (viewed from bottom)



-----Module Card Edge-----

MODULE SIGNAL PIN DESCRIPTIONS (compliant OSFP MSA Rev 5.0)

Name	Direction	Description
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receiver differential pairs from module to host.

RX[8:1]n	output	
SCL	Bi-direction	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	Bi-direction	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	Bi-direction	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in Section 10.5.3
INT/RSTn	Bi-direction	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in Section 10.5.2
VCC	power	3.3V power for module.
GND	ground	Module Ground. Logic and power return path.

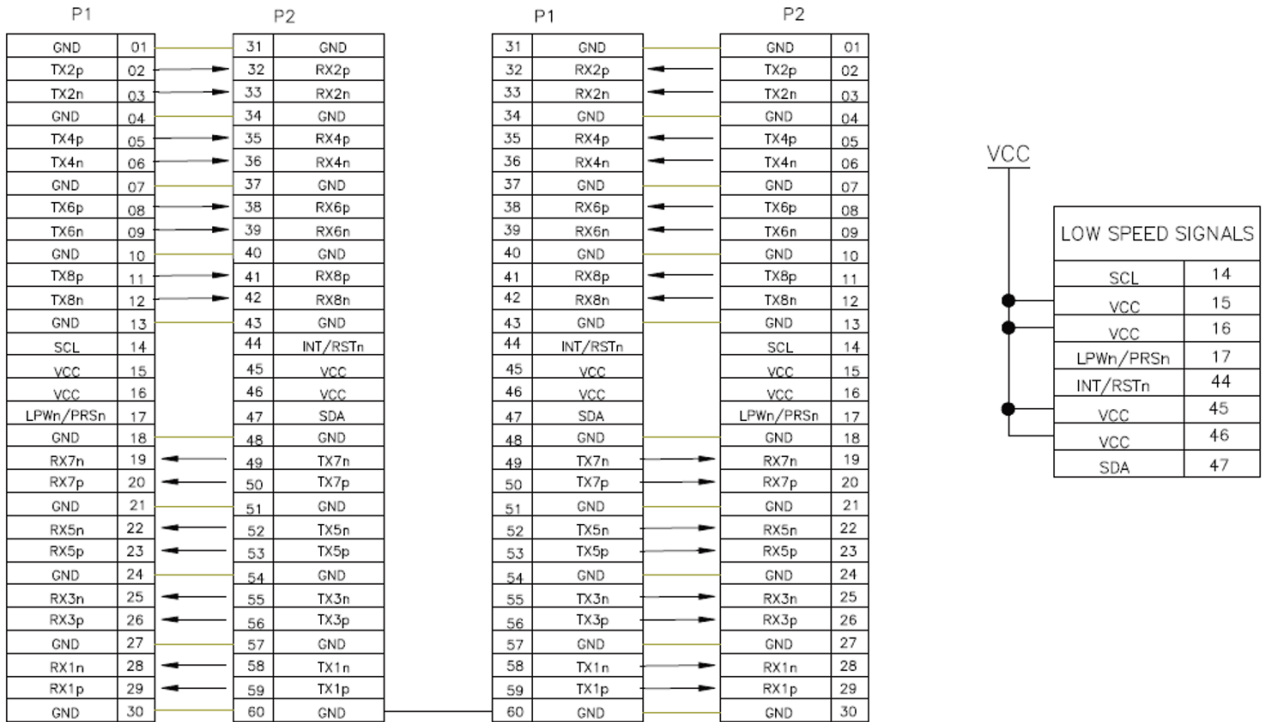
MODULE PIN LISTS (compliant OSFP MSA Rev 5.0)

PIN	Symbol	Description	Plug Sequence
1	GND	Ground	1
2	TX2p	Transmitter Data Non-Inverted	3
3	TX2n	Transmitter Data Inverted	3
4	GND	Ground	1
5	TX4p	Transmitter Data Non-Inverted	3
6	TX4n	Transmitter Data Inverted	3
7	GND	Ground	1
8	TX6p	Transmitter Data Non-Inverted	3
9	TX6n	Transmitter Data Inverted	3
10	GND	Ground	1
11	TX8p	Transmitter Data Non-Inverted	3
12	TX8n	Transmitter Data Inverted	3
13	GND	Ground	1
14	SCL	2-wire Serial interface clock	3
15	VCC	+3.3V Power supply	2
16	VCC	+3.3V Power supply	2

17	LPWn/PRSn	Low-Power Mode / Module Present	3
18	GND	Ground	1
19	RX7n	Receiver Data Inverted	3
20	RX7p	Receiver Data Non-Inverted	3
21	GND	Ground	1
22	RX5n	Receiver Data Inverted	3
23	RX5p	Receiver Data Non-Inverted	3
24	GND	Ground	1
25	RX3n	Receiver Data Inverted	3
26	RX3p	Receiver Data Non-Inverted	3
27	GND	Ground	1
28	RX1n	Receiver Data Inverted	3
29	RX1p	Receiver Data Non-Inverted	3
30	GND	Ground	1
31	GND	Ground	1
32	RX2n	Receiver Data Inverted	3
33	RX2p	Receiver Data Non-Inverted	3
34	GND	Ground	1
35	RX4n	Receiver Data Inverted	3
36	RX4p	Receiver Data Non-Inverted	3
37	GND	Ground	1
38	RX6n	Receiver Data Inverted	3
39	RX6p	Receiver Data Non-Inverted	3
40	GND	Ground	1
41	RX8n	Receiver Data Inverted	3
42	RX8p	Receiver Data Non-Inverted	3
43	GND	Ground	1
44	INT/RSTn	Module Interrupt / Module Reset	3

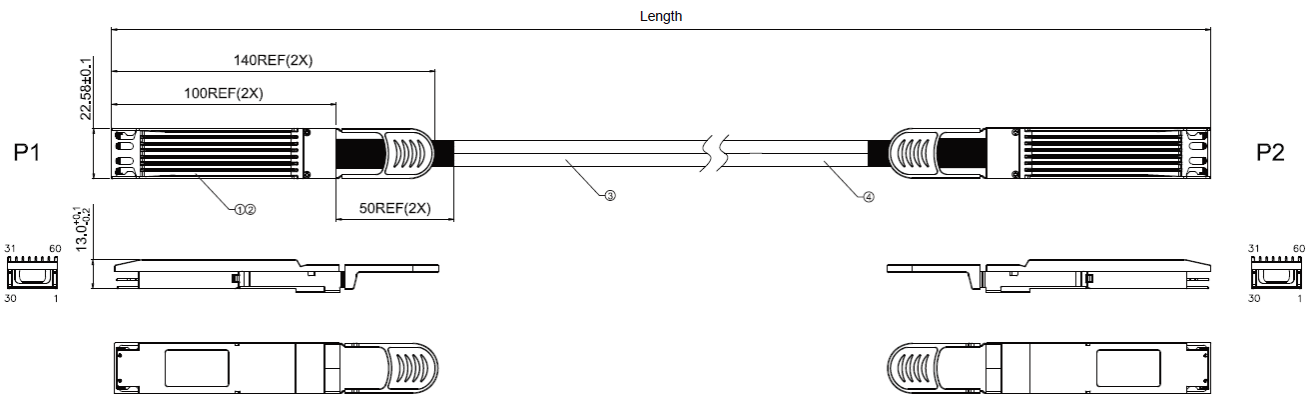
45	VCC	+3.3V Power supply	2
46	VCC	+3.3V Power supply	2
47	SDA	2-wire Serial interface data	3
48	GND	Ground	1
49	TX7p	Transmitter Data Non-Inverted	3
50	TX7n	Transmitter Data Inverted	3
51	GND	Ground	1
52	TX5p	Transmitter Data Non-Inverted	3
53	TX5n	Transmitter Data Inverted	3
54	GND	Ground	1
55	TX3p	Transmitter Data Non-Inverted	3
56	TX3n	Transmitter Data Inverted	3
57	GND	Ground	1
58	TX1p	Transmitter Data Non-Inverted	3
59	TX1n	Transmitter Data Inverted	3
60	GND	Ground	1

Wiring Diagram

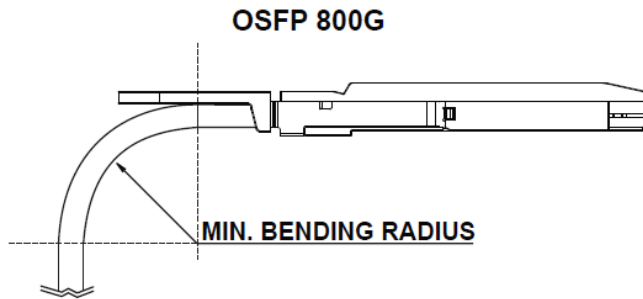


OSFP GND GROUP:
01/04/07/10/13/18/21/24/27/30/31/34/37/40/43/48/51/54/57/60

Mechanical Design Diagram



Bending Radius:



Min. bending radius allowed	Repeated	Single
	10 x ϕ	5 x ϕ

Ordering Information

Part No	Specification				
	Package	Data rate per Lane	Temp.	Gauge	Length
WS-OS8-DACP0-0H	OSFP to OSFP	53.125 GBd PAM4	-40~85 °C	30 AWG	0.5 m \pm 0.05 m
WS-OS8-DACP6-1	OSFP to OSFP	53.125 GBd PAM4	-40~85 °C	26 AWG	1.0 m \pm 0.05 m
WS-OS8-DACP6-1H	OSFP to OSFP	53.125 GBd PAM4	-40~85 °C	26 AWG	1.5 m \pm 0.05 m
WS-OS8-DACP6-2	OSFP to OSFP	53.125 GBd PAM4	-40~85 °C	26 AWG	2.0 m \pm 0.05 m

Modification History

Revision	Date	Description	Originator	Reviewed by	Approved by
V1.0	15-Oct-2024	New Issue	Ken Chang	Wayne Liao	Tom Tang



Headquarters
6 F., No. 57, Nanxing Rd., Xizhi Dist., New Taipei
City 221026, Taiwan
Tel: +886-2-2698-7208
Fax: +886-2-2698-7210
Email: sales@wavesplitter.com
Website: <https://wavesplitter.com/>