WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

# 800G OSFP to 2x QSFP112 Breakout AOC
# P/N: WS-O82Q-AOCxCyy4

## Features:

- Supports 800 Gb/s aggregate data rate
  (8 × 106.25 Gb/s PAM4)
- OSFP to 2 × QSFP112 breakout Active Optical Cable
- OSFP compliant with OSFP MSA (Type 2, Close-top)
- QSFP112 compliant with QSFP112 MSA
- Electrical interface compliant with IEEE 802.3df:
  800GAUI-8 (OSFP side)
  400GAUI-4 (QSFP side)
- Supports CMIS Rev. 5.0 or later
- Link Distance up to 50 m via OM4 MMF
- Power consumption:
  Max. 15 W (OSFP end)
  Max. 8.5 W per QSFP end
- Single 3.3 V power supply
- Operating case temperature: 0 °C to 70 °C
- RoHS compliant
- Class 1 laser safety compliant

## Standard:

- IEEE 802.3df 800GAUI-8 and 400GAUI-4
- OSFP MSA
- QSFP112 MSA
- CMIS Rev. 5.0 or later

## Applications:

- 800G Ethernet data center interconnects
- OSFP to QSFP112 breakout links
- High-density switch and router connections
- Cloud and hyperscale data center networking

## *Description*

The 800G OSFP to 2×400G QSFP112 Active Optical Cable (AOC) is designed for high-speed data center interconnect applications. It supports an aggregate data rate of 800 Gb/s using 8 lanes of 106.25 Gb/s PAM4 signaling on the OSFP side and splits into two independent 400 Gb/s QSFP112 interfaces up to 50 m via OM4 fiber. Optical performance is compliant with IEEE 802.3df specifications for VR4 interfaces.

The product integrates optical engines and electrical interfaces within cable assemblies to provide low power consumption, high reliability, and simplified system integration for short-reach interconnects.

## *Absolute Maximum Ratings*

| Parameter | Symbol | Min. | Max. | Unit. | Notes. |
|---|---|---|---|---|---|
| Storage Temperature | $T_{sto}$ | -40 | 85 | ℃ | |
| Supply Voltage | $V_{cc}$ | -0.5 | 3.6 | V | |
| Relative Humidity | RH | 5 | 85 | % | Non-condensing |
| Damage Threshold, each lane | | 5 | | dBm | |

## *Recommended Operating Conditions*

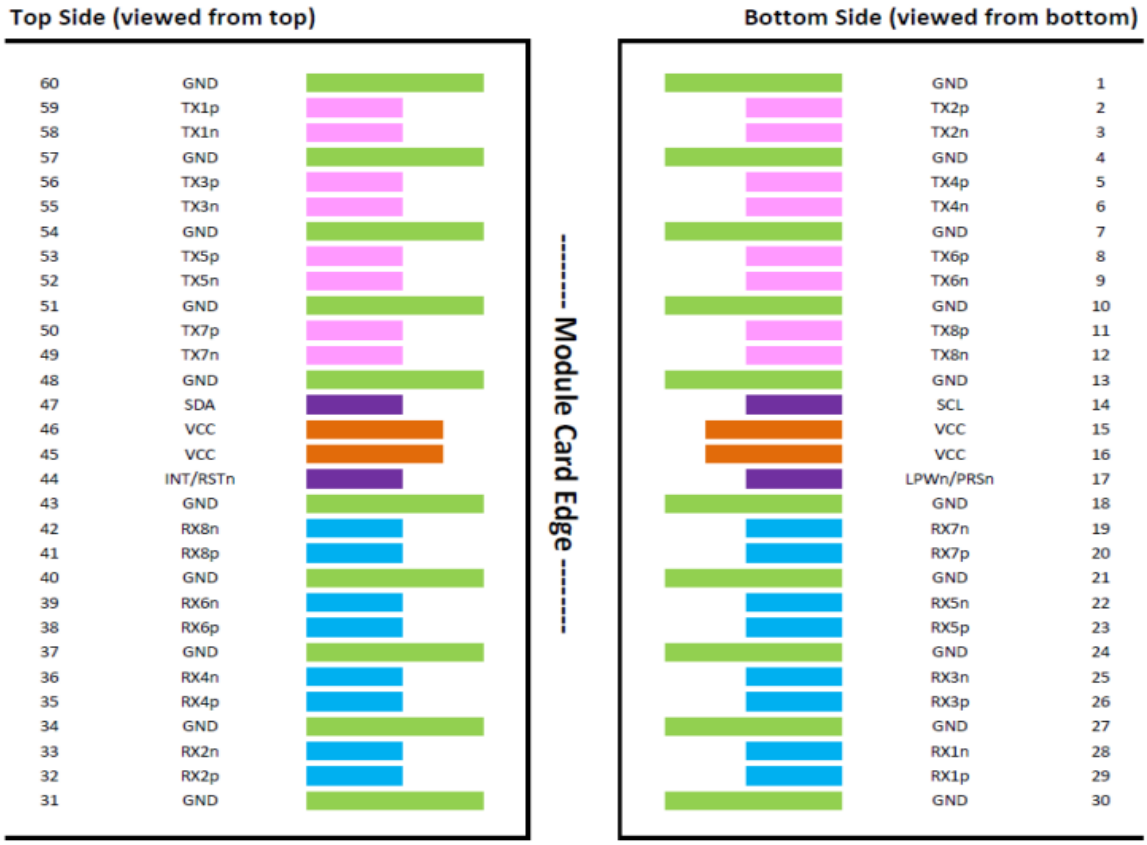
| Parameter | Symbol | Min. | Typ. | Max. | Unit. | Notes. |
|---|---|---|---|---|---|---|
| Operating Case Temperature | $T_C$ | 0 | | 70 | °C | |
| Power Supply Voltage | Vcc | 3.135 | 3.3 | 3.465 | V | |
| Power Dissipation per OSFP | Pd | | | 15 | W | 1 |
| Power Dissipation per QSFP112 | Pd | | | 8.5 | W | 1 |
| Bit Rate per channel | BR | | 53.125 | | GBaud | PAM4 |

Note:
1 Per terminal

## *Electrical Specification High Speed Signal*

| Parameter | Symbol / Test Point | Min. | Typ. | Max. | Unit. | Notes |
|---|---|---|---|---|---|---|
| Pre-FEC BER | $BER_{pre}$ | | | 1E-6 | | |
| Post-FEC BER | $BER_{pos}$ | | | 1E-12 | | KP4 |
| Signaling Rate per Lane | SRL | | 53.125 | | GBaud | |
| AC common-mode output Voltage (RMS) | TP4 | | | 25 | mV | |
| Differential output Voltage (Long mode) | TP4 | | | 845 | mV | |
| Differential output Voltage (Short mode) | TP4 | | | 600 | mV | |
| Eye height | TP4 | 15 | | | mV | |
| Differential Termination Mismatch | TP1, TP4 | | | 10 | % | |
| Transition Time (min, 20% to 80%) | TP4 | 8.5 | | | ps | |
| DC common mode Voltage | TP1, TP4 | -350 | | 2850 | mV | |

## *Pin Assignment of OSFP*



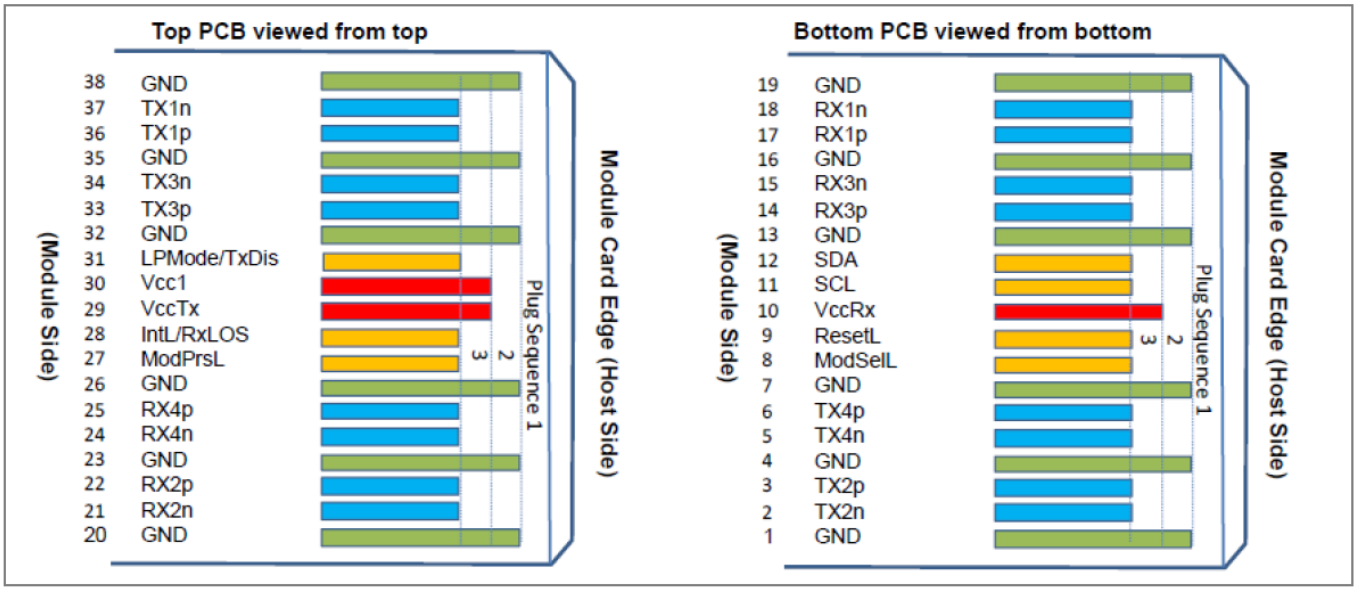

**Pin out of Connector Block on Host Board**

| Name | Direction | Description |
|---|---|---|
| TX[8:1]p | input | Transmit differential pairs from host to module. |
| TX[8:1]n | input | |
| RX[8:1]p | output | Receive differential pairs from host to module. |
| RX[8:1]n | output | |
| SCL | bidir | 2-wire serial clock signal. Requires pull-up resistor to 3.3V on host. |
| SDA | bidir | 2-wire serial data signal. Requires pull-up resistor to 3.3V on host. |
| LPWn/PRSn | bidir | Multi level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in the OSFP Specification. |
| INT/RSTn | bidir | Multi level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in OSFP Specification. |
| VCC | power | 3.3V power for module. |
| GND | ground | Module Ground. Logic and power return path. |

| Pin | Logic | Symbol | Description | Notes |
|---|---|---|---|---|
| 1 | GND | | Ground | |
| 2 | TX2p | CML-I | Transmitter Data Non-Inverted | |
| 3 | TX2n | CML-I | Transmitter Data Inverted | |
| 4 | GND | | Ground | |
| 5 | TX4p | CML-I | Transmitter Data Non-Inverted | |
| 6 | TX4n | CML-I | Transmitter Data Inverted | |
| 7 | GND | | Ground | |
| 8 | TX6p | CML-I | Transmitter Data Non-Inverted | |
| 9 | TX6n | CML-I | Transmitter Data Inverted | |
| 10 | GND | | Ground | |
| 11 | TX8p | CML-I | Transmitter Data Non-Inverted | |
| 12 | TX8n | CML-I | Transmitter Data Inverted | |
| 13 | GND | | Ground | |
| 14 | SCL | LVCMOS-I/O | 2-wire Serial interface clock | |
| 15 | VCC | | +3.3V Power | |
| 16 | VCC | | +3.3V Power | |
| 17 | LPWn/PRSn | Multi-Level | Low-Power Mode / Module Present | |
| 18 | GND | | Ground | |
| 19 | RX7n | CML-O | Receiver Data Inverted | |
| 20 | RX7p | CML-O | Receiver Data Non-Inverted | |
| 21 | GND | | Ground | |
| 22 | RX5n | CML-O | Receiver Data Inverted | |
| 23 | RX5p | CML-O | Receiver Data Non-Inverted | |
| 24 | GND | | Ground | |
| 25 | RX3n | CML-O | Receiver Data Inverted | |
| 26 | RX3p | CML-O | Receiver Data Non-Inverted | |
| 27 | GND | | Ground | |
| 28 | RX1n | CML-O | Receiver Data Inverted | |
| 29 | RX1p | | Receiver Data Non-Inverted | |
| 30 | GND | | Ground | |
| 31 | GND | | Ground | |
| 32 | RX2p | CML-O | Receiver Data Non-Inverted | |

| | | | | |
|---|---|---|---|---|
| 33 | RX2n | CML-O | Receiver Data Inverted | |
| 34 | GND | | Ground | |
| 35 | RX4p | CML-O | Receiver Data Non-Inverted | |
| 36 | RX4n | CML-O | Receiver Data Inverted | |
| 37 | GND | | Ground | |
| 38 | RX6p | CML-O | Receiver Data Non-Inverted | |
| 39 | RX6n | CML-O | Receiver Data Inverted | |
| 40 | GND | | Ground | |
| 41 | RX8p | CML-O | Receiver Data Non-Inverted | |
| 42 | RX8n | CML-O | Receiver Data Inverted | |
| 43 | GND | | Ground | |
| 44 | INT/RSTn | Multi-Level | Module Interrupt / Module Reset | |
| 45 | VCC | | +3.3V Power | |
| 46 | VCC | | +3.3V Power | |
| 47 | SDA | LVCMOS-I/O | 2-wire Serial interface data | |
| 48 | GND | | Ground | |
| 49 | TX7n | CML-I | Transmitter Data Inverted | |
| 50 | TX7p | CML-I | Transmitter Data Non-Inverted | |
| 51 | GND | | Ground | |
| 52 | TX5n | CML-I | Transmitter Data Inverted | |
| 53 | TX5p | CML-I | Transmitter Data Non-Inverted | |
| 54 | GND | | Ground | |
| 55 | TX3n | CML-I | Transmitter Data Inverted | |
| 56 | TX3p | CML-I | Transmitter Data Non-Inverted | |
| 57 | GND | | Ground | |
| 58 | TX1n | CML-I | Transmitter Data Inverted | |
| 59 | TX1p | CML-I | Transmitter Data Non-Inverted | |
| 60 | GND | | Ground | |

## *Pin Descriptions of QSFP112*




***Pin out of Connector Block on Host Board***

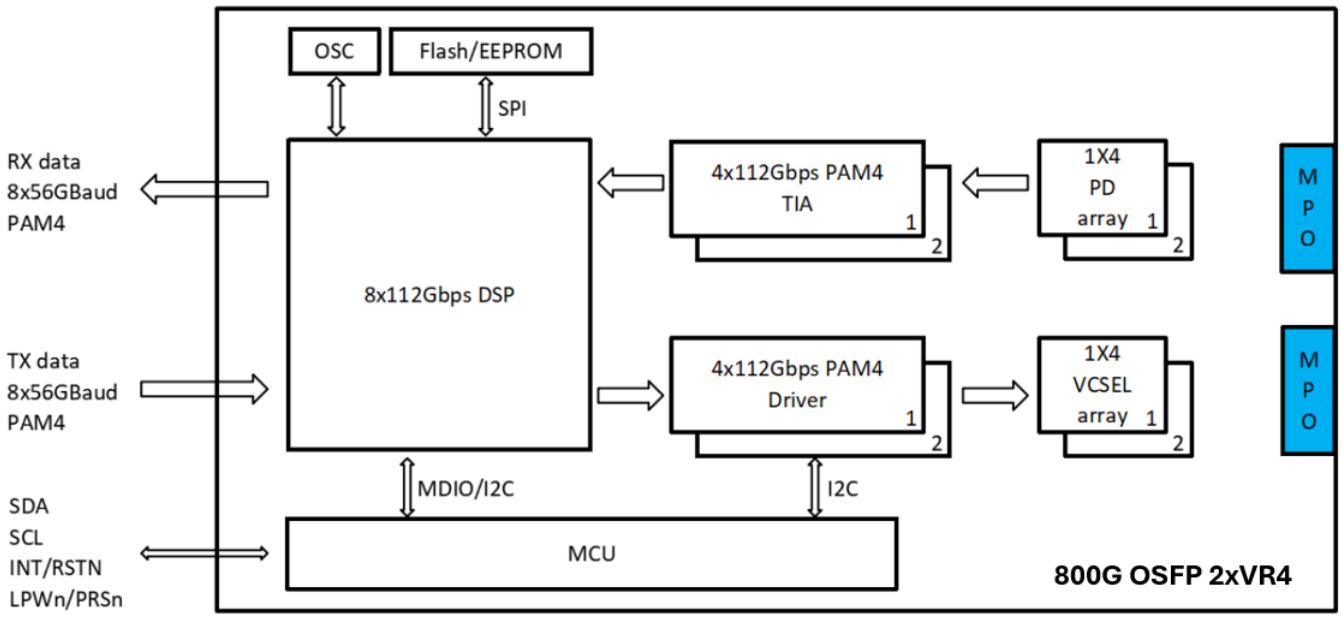
| PIN | Logic | Symbol | Description | Plug Sequence | Notes |
|---|---|---|---|---|---|
| 1 | | GND | Ground | 1 | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3 | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3 | |
| 4 | | GND | Ground | 1 | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3 | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3 | |
| 7 | | GND | Ground | 1 | 1 |
| 8 | LVTTL-I | ModselL | Module Select | 3 | |
| 9 | LVTTL-I | ResetL | Module Reset | 3 | |
| 10 | | Vcc Rx | +3.3V Power Supply Receiver | 2 | 2 |
| 11 | LVCMOS-I/O | SCL | 2-wire serial interface clock | 3 | |
| 12 | LVCMOS-I/O | SDA | 2-wire serial interface data | 3 | |
| 13 | | GND | Ground | 1 | 1 |

| | | | | | |
|---|---|---|---|---|---|
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3 | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3 | |
| 16 | | GND | Ground | 1 | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3 | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3 | |
| 19 | | GND | Ground | 1 | 1 |
| 20 | | GND | Ground | 1 | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3 | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3 | |
| 23 | | GND | Ground | 1 | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3 | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3 | |
| 26 | | GND | Ground | 1 | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | 3 | |
| 28 | LVTTL-O | IntL/RxLOSL | Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636). Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636). | 3 | |
| 29 | | Vcc Tx | +3.3V Power supply transmitter | 2 | 2 |
| 30 | | Vcc1 | +3.3V Power supply | 2 | 2 |
| 31 | LVTTL-I | LPMode/TxDis | Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636). | 3 | |
| 32 | | GND | Ground | 1 | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3 | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3 | |
| 35 | | GND | Ground | 1 | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3 | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3 | |
| 38 | | GND | Ground | 1 | 1 |

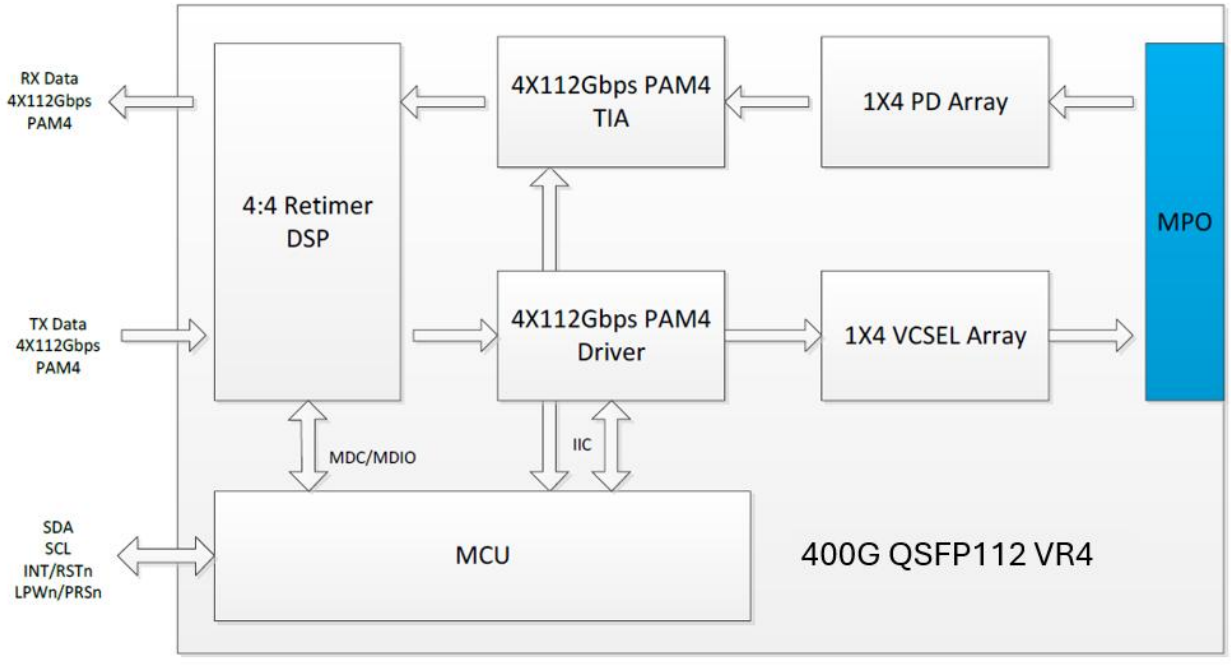
Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements, defined for the host side of the Host Edge Card Connector, are listed in Table 4. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

## *Transceiver Module Block Diagram*




OSFP SIDE

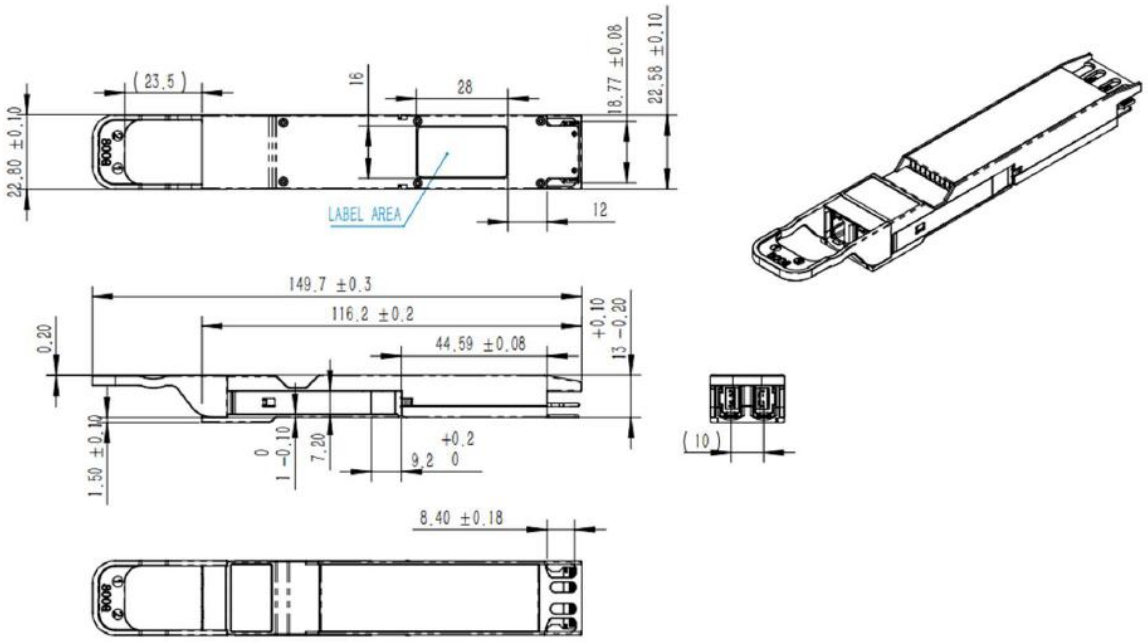



QSFP112 SIDE

***Mechanical Drawing***

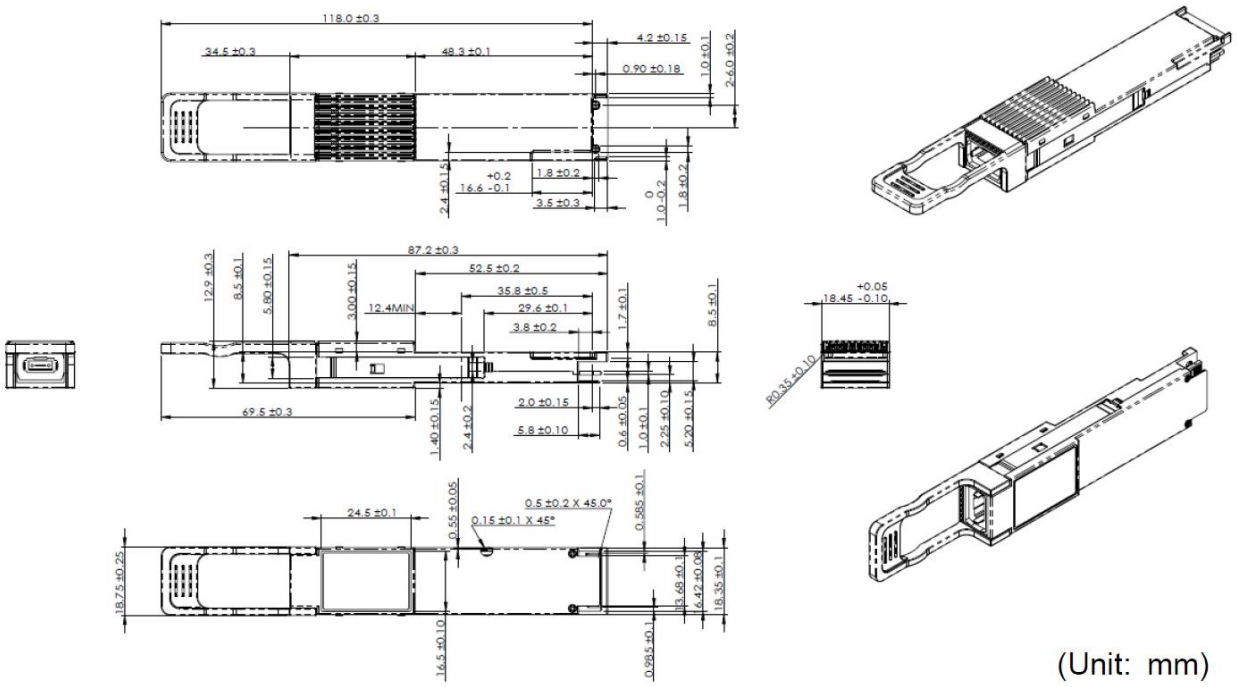
a. OSFP

Reference to OSFP Type2 Close-top




Unit: mm

b. QSFP112




**Cable Length**

| Cable Length (Unit: m) | Tolerant (Unit: cm) |
|---|---|
| ＜1.0 | +5/-0 |
| 1.0~4.5 | +15/-0 |
| 5.0~14.5 | +30/-0 |
| ≥15.0 | +2%/-0 |

**Cable Diameter: 3.0mm**

**Minimum bending radius: 30mm**

## *Ordering Information*

| Part No | Specification | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Package | Data rate | Laser | Fiber | Cable Type | Cable Length | Temp. | Application |
| WS-O82Q-AOCXC014 | OSFP to QSFP112 | 800 Gbps | 850 nm VCSEL | OM4 | Round LSZH, OFNP, or OFNR | 1 m | 0~70°C | 800GbE to 2x400GbE |
| WS-O82Q-AOCXC034 | OSFP to QSFP112 | 800 Gbps | 850 nm VCSEL | OM4 | Round LSZH, OFNP, or OFNR | 3 m | 0~70°C | 800GbE to 2x400GbE |
| WS-O82Q-AOCXC054 | OSFP to QSFP112 | 800 Gbps | 850 nm VCSEL | OM4 | Round LSZH, OFNP, or OFNR | 5 m | 0~70°C | 800GbE to 2x400GbE |
| WS-O82Q-AOCXC104 | OSFP to QSFP112 | 800 Gbps | 850 nm VCSEL | OM4 | Round LSZH, OFNP, or OFNR | 10 m | 0~70°C | 800GbE to 2x400GbE |
| WS-O82Q-AOCXC154 | OSFP to QSFP112 | 800 Gbps | 850 nm VCSEL | OM4 | Round LSZH, OFNP, or OFNR | 15 m | 0~70°C | 800GbE to 2x400GbE |
| WS-O82Q-AOCxCyy4 | OSFP to QSFP112 | 800 Gbps | 850 nm VCSEL | OM4 | Round LSZH, Round OFNP, Round OFNR | yy m | 0~70°C | 800GbE to 2x400GbE |

Note:

Cable jacket type: x= L for LSZH, P for OFNP, and R for OFNR, X for any of the above (OFNR, OFNP, or LSZH)

Length: yy meters

Variant Length and Cable Types can be customized. Please contact our sales for detail information

## *Modification History*

| Revision | Date | Description | Originator | Review | Approved |
|---|---|---|---|---|---|
| V1.0 | 19-Feb-2025 | New Issue | Ken Cheng | Joanne Ni | Tom Tang |

WAVESPLITTER TECHNOLOGIES, INC.

**Headquarters**
16F-5, No. 75, Sec. 1, Xintai 5th Rd., Xizhi Dist.,
New Taipei City 22101, Taiwan
Tel: +886-2-2698-7208
Fax: +886-2-2698-7210
Email: sales@wavesplitter.com
Website: https://wavesplitter.com/