WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

40GBase QSFP+ LR4 10km transceiver
P/N: WST-QSFP+LR4-C

Features:

- Hot Pluggable QSFP+ form factor
- DFB Laser/PIN Photo Detector
- Supports 10.3125Gb/s per channel
- Maximum power consumption 3.5W
- Up to 10km transmission on SMF
- Operating Case Temperature: 0℃~70℃
- Duplex LC receptacles
- SFF-8636: Management Interface
- SFF-8661: Pluggable Module
- SFF-8679: General Electrical
- GR-468: Reliability Qualification
- IEEE 802.3ba: Physical Layer Specifications and Management Parameters
- ROHS-6: Environment Safety

Applications:

- Ethernet for 40GBASE-LR4
- InfiniBand EDR, FDR

General Product Characteristics

Parameter	Value	Unit	Comments
Module Form Factor	QSFP+	As defined by SFF-8661	Module Form Factor
Number of Lanes	4 TX and 4 RX		
Maximum Aggregate Data Rate	41.25	Gb/s	
Maximum Data Rate per Lane	10.3125	Gb/s	
Protocols Supported	InfiniBand, Ethernet		
Electrical Interface and Pin-out	38-pin edge connector		Pin-out as defined by SFF-8679
Maximum Power Consumption	3.5	Watts	Varies with output voltage swing and pre-emphasis settings
Management Interface	Serial, I^2C-based, 400 kHz maximum frequency		As defined by SFF-8636

Absolute Maximum Parameters

Exceeding the limits below may damage the optical transceiver module permanently

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
Maximum Supply Voltage	V_{cc}	-0.5		3.6	V	
Storage Temperature	T_{sto}	-40		85	°C	
Case Operating Temperature	T_{op}	0		70	°C	
Relative Humidity	RH	0		85	%	1

Note:

1. No-condensing.

Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
Supply Voltage	V_{cc}	3.13		3.47	V	
Power Consumption	P_{Con}			3.5	W	
Bit Rate	BR		10.3125		Gb/s	1
Transmit Distance	D	-		10	km	2
Number of Lanes		4				
Management Interface		Serial, I^2C-based, maximum frequency 400 kHz				3
Logic Input Voltage High	V_{ih}	2		Vcc+0.3	V	
Logic Input Voltage Low	V_{il}	-0.3		0.8	V	

Note:

1. Single lane
2. As defined by IEEE802.3ba
3. As defined by SFF-8636

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Transceiver Power Supply Current	I_{cc}			1100	mA	
Transceiver Power On Initialization Time	T_{init}			2000	ms	
Transmitter at TP1a						
Differential Data Input Voltage Peak to Peak Swing	$V_{in,pp}$	200		1200	mV	
Differential Input Impedance	Zin	90	100	110	Ohms	
Differential Input Return Loss	SDD11	$< -12 + 2 \times SQRT(f), f$ in GHz			dB	0.01-4.1GHz
		$< -6.3 + 13 \times \log_{10}\left(\frac{f}{5.5}\right), f\ in\ GHz$			dB	4.1-11.1GHz
Differential to Common Mode Loss	SCD11			-10	dB	0.01-11.1GHz
Jitter Tolerance (Total)	TJ			0.4	UI	
Jitter Tolerance (Deterministic)	DJ			0.15	UI	
Receiver at TP4						
Differential Data Output Voltage Peak to Peak Swing	V_{opp}	300		800	mV	
Differential Output Impedance	Zout	90	100	110	Ohms	
Differential Output Return Loss	SDD22	$< -12 + 2 \times SQRT(f), f$ in GHz			dB	0.01-4.1GHz
		$< -6.3 + 13 \times \log_{10}\left(\frac{f}{5.5}\right), f\ in\ GHz$			dB	4.1-11.1GHz
Common Mode Output Return Loss	SCC22	$< -7 + 1.6 \times f, f$ in GHz			dB	0.01-2.5GHz
				-3	dB	2.5-11.1GHz
Output Rise and Fall time (20% to 80%)	T_r, T_f	24			ps	
Deterministic Jitter	DJ_{out}			0.38	UI	
Total Jitter	TJ_{out}			0.64	UI	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
Transmitter						
Signaling Speed per Lane		10.3125 ± 100ppm			Gb/s	
Lane wavelengths (Range)	λ	1264.5	1271	1277.5	nm	
		1284.5	1291	1297.5		
		1304.5	1311	1317.5		
		1324.5	1331	1337.5		
Side-mode suppression ratio	SMSR	30			dB	
Average launch power, each lane	P_{avg}	-7		2.3	dBm	
Optical Modulation Amplitude	OMA	-4		3.5	dBm	
Extinction ratio	ER	3.5			dB	
Transmitter and dispersion penalty, each lane	TDP	-2.3			dB	
Average launch power of OFF transmitter, each lane	P_{off}			-30	dBm	
Transmitter eye mask definition		Compliant with IEEE 802.3ba				1
Receiver						
Signaling Speed per Lane		10.3125±100ppm			Gb/s	
Lane wavelengths (Range)	λ	1260	1310	1360	nm	
Average receiver power, each lane		-13.7		3	dBm	2
OMA Sensitivity power, each lane				-11.5		2
Receiver overload		4.5			dBm	
Reflectance	Ref			-26	dB	

Notes:

1. Measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps for Hit ratio<$5x10^{-5}$
2. Measured with conformance test signal for BER=$1x10^{-12}$

Pin Description

Top side
Viewed from Top

Bottom side
Viewed from Bottom

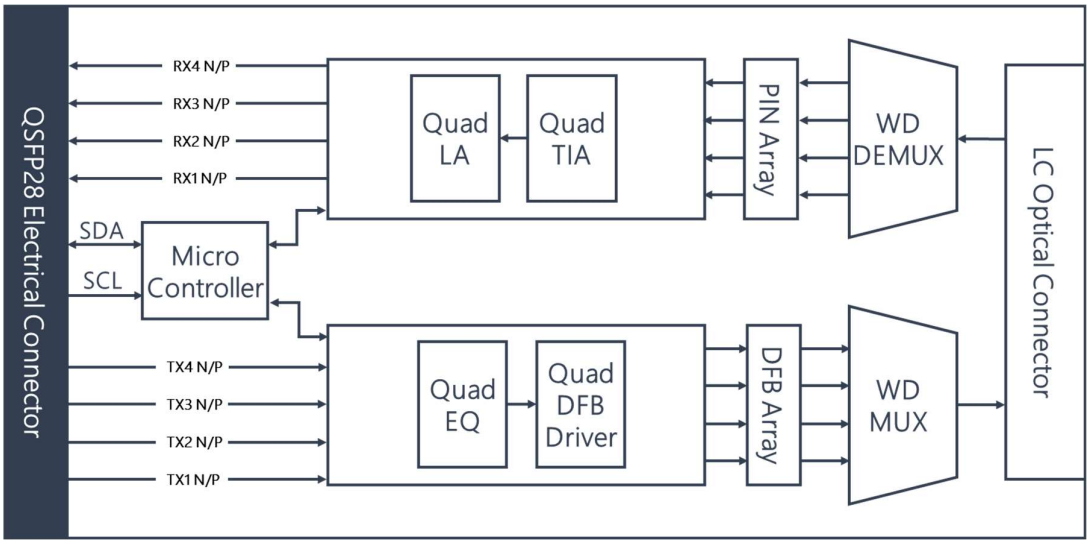
PIN	Symbol	Description	Note
1	GND	Ground	
2	TX2n	Transmitter Inverted Data Input	
3	TX2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	TX4n	Transmitter Inverted Data Input	
6	TX4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	2
9	ResetL	Module Reset	2
10	V_{cc} RX	+3.3V Receiver Power Supply Receiver	
11	SCL	2-wire Serial Interface Clock	2
12	SDA	2-wire Serial Interface Data	2
13	GND	Ground	1
14	RX3p	Receiver Non-Inverted Data Output	
15	RX3n	Receiver Inverted Data Output	
16	GND	Ground	1

17	RX1p	Receiver Non-Inverted Data Output	
18	RX1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	RX2n	Receiver Inverted Data Output	
22	RX2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	RX4n	Receiver Inverted Data Output	
25	RX4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present, internal pulled down to GND	
28	IntL	Interrupt output, should be pulled up on host board	
29	Vcc TX	+3.3V Transmitter Power Supply	
30	Vcc1	+3.3V Power Supply	
31	LPMode	Low Power Mode	2
32	GND	Ground	
33	TX3p	Transmitter Non-Inverted Data Input	
34	TX3n	Transmitter Inverted Data Input	
35	GND	Ground	
36	TX1p	Transmitter Non-Inverted Data Input	
37	TX1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are reference to this potential unless otherwise noted. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector, should be pulled up with 4.7~10K ohms on the host board to a voltage between 3.15V and 3.6V.

Recommended Host Board Schematic



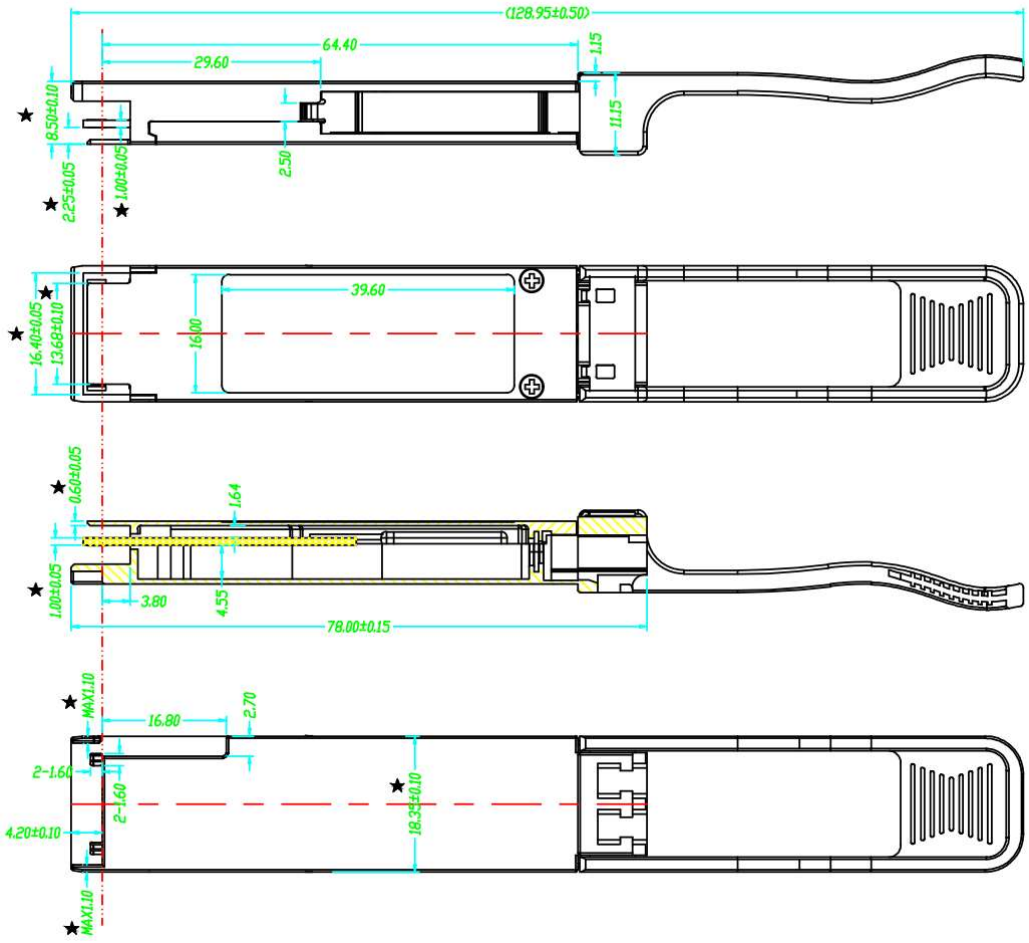
Memory Map

	2-Wire Serial Address 1010000x
	Lower Page 00h
0	Identifier
1 - 2	Status
3 - 2 1	Interrupt Flags
2 2 - 2 3	Free Side Device Monitors
3 4 - 8 1	Channel Monitors
8 2 - 8 5	Reserved
8 6 - 9 8	Control
99	Reserved
100-104	Hardware Interrupt Pin Masks
105-106	Vendor Specific
107	Reserved
108-110	Free Side Device Properties
111-112	Assigned for use by PCI Express
113	Free Side Device Properties
114-118	Reserved
119-122	Password Change Entry Area (Optional)
123-126	Password Entry Area (Optional)
127	Page Select Byte

	Optional	Optional	Optional
Upper Page 00h	Page 01h	Page 02h	Page 03h
128 Identifier	128 CC_APPS	128-255 User EEPROM data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		
	130-131 Application Code Entry 0		
	132-133 Application Code Entry 1		
192-223 Extended ID	134-253 other entries		176-223 Channel Thresholds
224-255 Vendor Specific ID			224 TX EQ & RX Emphasis Magnitude ID
			225 RX output amplitude indicators
			226-241 Channel Monitor Masks
	254-255 Application Code Entry TL		252-255 Reserved

Mechanical Design Diagram

Product shall be of design, construction and physical dimensions specified on applicable product drawing.



Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate per Lane	Laser	Optical Power	Detector	Max. Receive Sensitivity (OMA)	Temp	Reach	Other	Application code
WST-QSFP+LR4-C	QSFP+	10.3125 Gbps per Channel	DFB	-7~ +2.3 each Channel	PIN	-11.5Bm each Channel	0~70°C	10km	DDM RoHS	40G Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	28-May-2020	New Issue	Ivy Chen	Ethan Huang	Wayne Liao

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