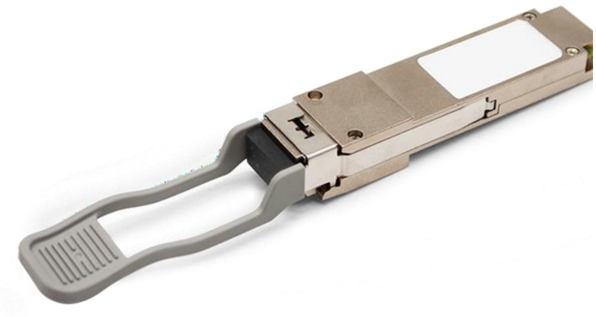
Data Sheet

100Gbps/40Gbps QSFP28 Bi-Directional Transceiver, 100m
P/N: WST-QS28-SRB-C



Features:

- Compliant to the 100GbE XLPPI electrical specification per IEEE 802.3bm
- Compliant to QSFP28 SFF-8636 Specification
- Aggregate bandwidth of > 100Gbps
- Supports 25.78125Gb/s, 10.3125Gb/s per channel
- Dual wavelength VCSEL bi-directional
- optical interface, PAM4 2 × 50-Gb/s 850nm/900 nm
- QSFP28 MSA compliant
- Capable of over 70m transmission on OM3 Multimode Fiber (MMF)and 100m on OM4 MMF
- Single +3.3V power supply operating
- With digital diagnostic functions
- Temperature range 0°C to 70°C

Applications:

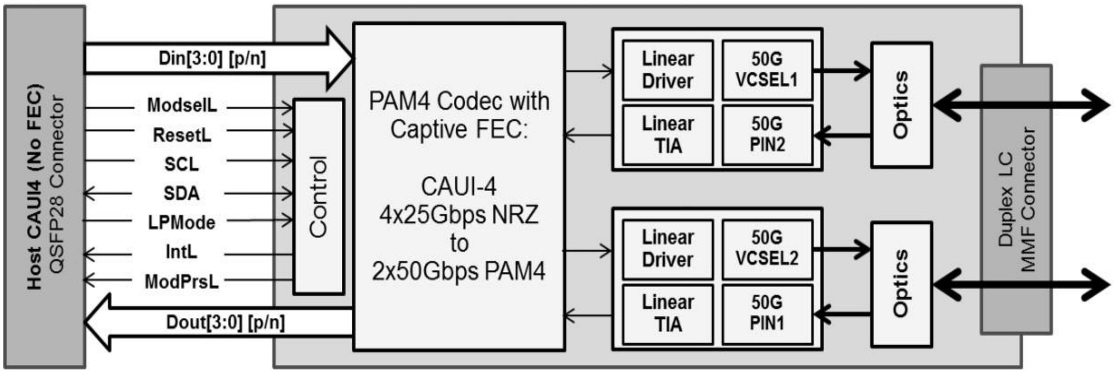
- 100 Gigabit Ethernet Interconnects
- 40 Gigabit Ethernet Interconnects
- Datacom/Telecom Switch & Router Connections
- Data Aggregation and Backplane Applications

Description

This product converts the 4-channel of 100Gbps aggregated NRZ electrical input data into one channel of 50Gbaud PAM4 optical signal (light) on 850nm/900nm center wavelength through a DSP based gearbox by VCSEL bi-directional.

The light propagates out of the transmitter into an MMF fiber. The receiver module accepts the 50Gbaud PAM4 optical signal input, and converts it into a 50Gbaud PAM4 electrical signal via a linear amplifier. And then convert the 50Gbaud PAM4 signal into 4 channels of 25Gbps NRZ signals. Figure "Transceiver Functional Diagram" shows the functional block diagram of this product.

Transceiver Block Diagram



Absolute Maximum Ratings

Data Rate Specifications	Symbol	Min	Typ.	Max	Unit
Storage Temperature	TS	-40		+85	°C
Supply Voltage	VCCT, R	-0.5		4	V
Relative Humidity	RH	0		85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Case operating Temperature	TC	0		+70	°C
Supply Voltage	VCCT, R	+3.13	3.3	+3.47	V
Supply Current	ICC			1000	mA
Power Dissipation	PD			3.5	W

Electrical Characteristics (TOP= 0 to 70 °C, V_{CC} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Data Rate per Channel			25.78125		Gbps	
			10.3125		Gbps	
Power Consumption			2.5	3.5	W	
Supply Current	Icc		0.75	1.0	A	
Control I/O Voltage-High	VIH	2.0		Vcc	V	
Control I/O Voltage-Low	VIL	0		0.7	V	
Inter-Channel Skew	TSK			150	Ps	
RESETL Duration			10		Us	
RESETL De-assert time				100	ms	
Power On Time				100	ms	
Transmitter						
Single Ended Output Voltage Tolerance		0.3		4	V	
Common mode Voltage Tolerance		15			mV	
Transmit Input Diff Voltage	VI	120		1200	mV	
Transmit Input Diff Impedance	ZIN	80	100	120		
Data Dependent Input Jitter	DDJ			0.1	UI	
Data Input Total Jitter	TJ			0.28	UI	
Receiver						
Single Ended Output Voltage Tolerance		0.3		4	V	
Rx Output Diff Voltage	Vo		600	800	mV	
Rx Output Rise and Fall Voltage	Tr/Tf	12			ps	1
Total Jitter	TJ			0.7	UI	
Deterministic Jitter	DJ			0.42	UI	

Notes:

1. 20～80%

Optical Characteristics (TOP = 0 to 70 °C, V_{CC} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Transmitter						
Optical Wavelength CH1	λ	832	850	868	nm	
Optical Wavelength CH2	λ	882	900	918	nm	
RMS Spectral Width	Pm		0.5	0.65	nm	
Average Optical Power per Channel	Pavg	-6	-1	+4.0	dBm	
Laser Off Power Per Channel	Poff			-30	dBm	
Optical Extinction Ratio	ER	3.0			dB	
Relative Intensity Noise	RIN			-128	dB/HZ	1
Optical Return Loss Tolerance				12	dB	
Receiver						
Optical Center Wavelength CH1	λ	882	900	918	nm	
Optical Center Wavelength CH2	λ	832	850	868	nm	
Receiver Sensitivity per Channel	R		-11		dBm	
Maximum Input Power	PMAX	+0.5			dBm	
Receiver Reflectance	Rrx			-12	dB	
LOS De-Assert	LOSD			-14	dBm	
LOS Assert	LOSA	-30			dBm	
LOS Hysteresis	LOSH	0.5			dB	

Notes:

1. 12dB Reflection

Pin Assignment

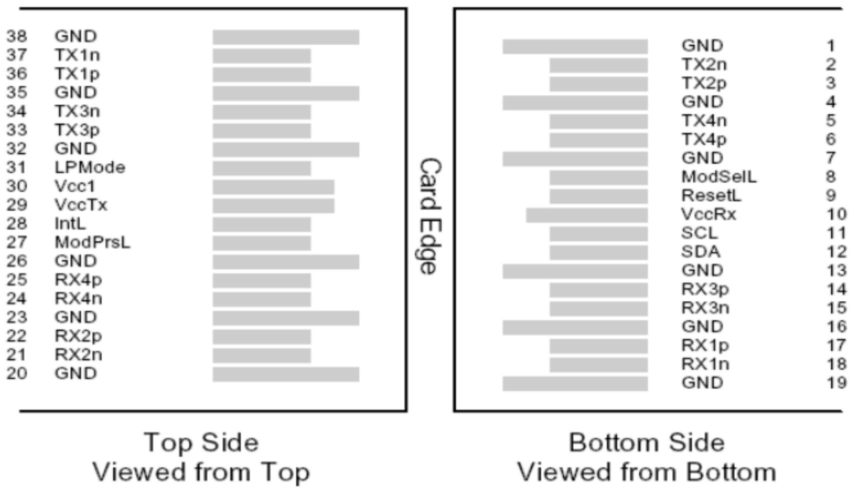


Diagram of Host Board Connector Block Pin Numbers and Name

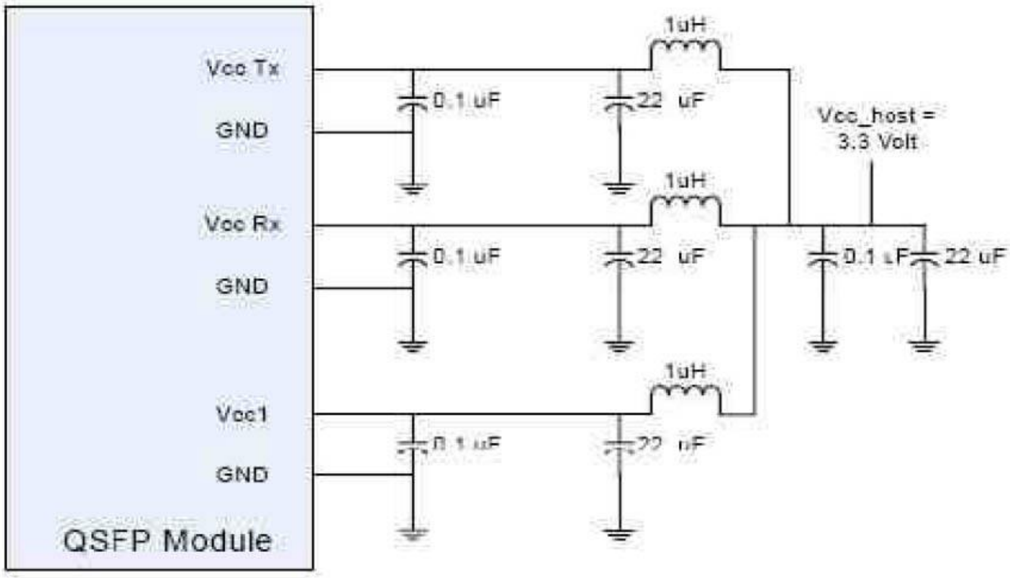
Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1

21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

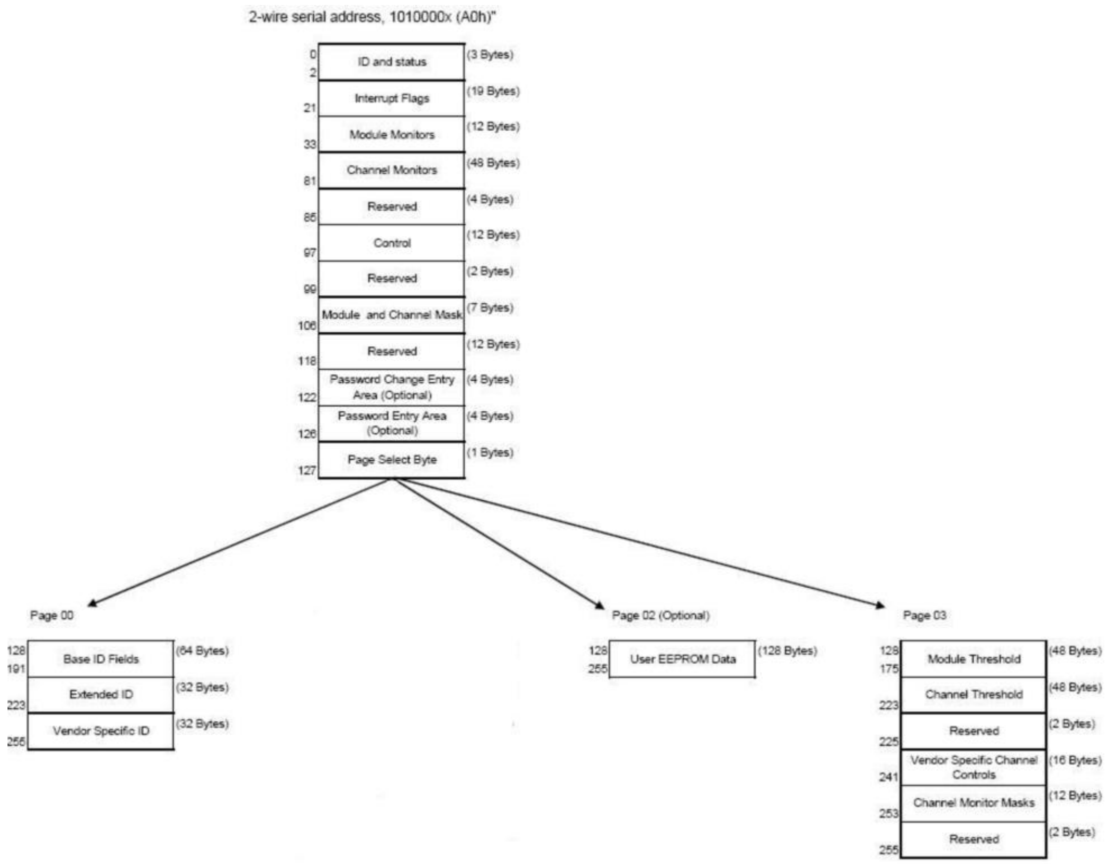
Notes:

1. GND is the symbol for single and supply(power) common for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

Recommended Circuit



Memory map



Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all QSFP+ SRBD. A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in flowing. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read /Write
86-97	Control (12 Bytes)	Read /Write
98-99	Reserved (2 Bytes)	Read /Write
100-106	Module and Channel Masks (7 Bytes)	Read /Write
107-118	Reserved (12 Bytes)	Read /Write
119-122	Reserved (4 Bytes)	Read /Write
123-126	Reserved (4 Bytes)	Read /Write
127	Page Select Byte	Read /Write
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read /Write
226-239	Reserved (14 Bytes)	Read /Write
240-241	Channel Controls (2 Bytes)	Read /Write

242-253	Reserved (12 Bytes)	Read /Write
254-255	Reserved (2 Bytes)	Read /Write

Timing for Soft Control and Status Functions

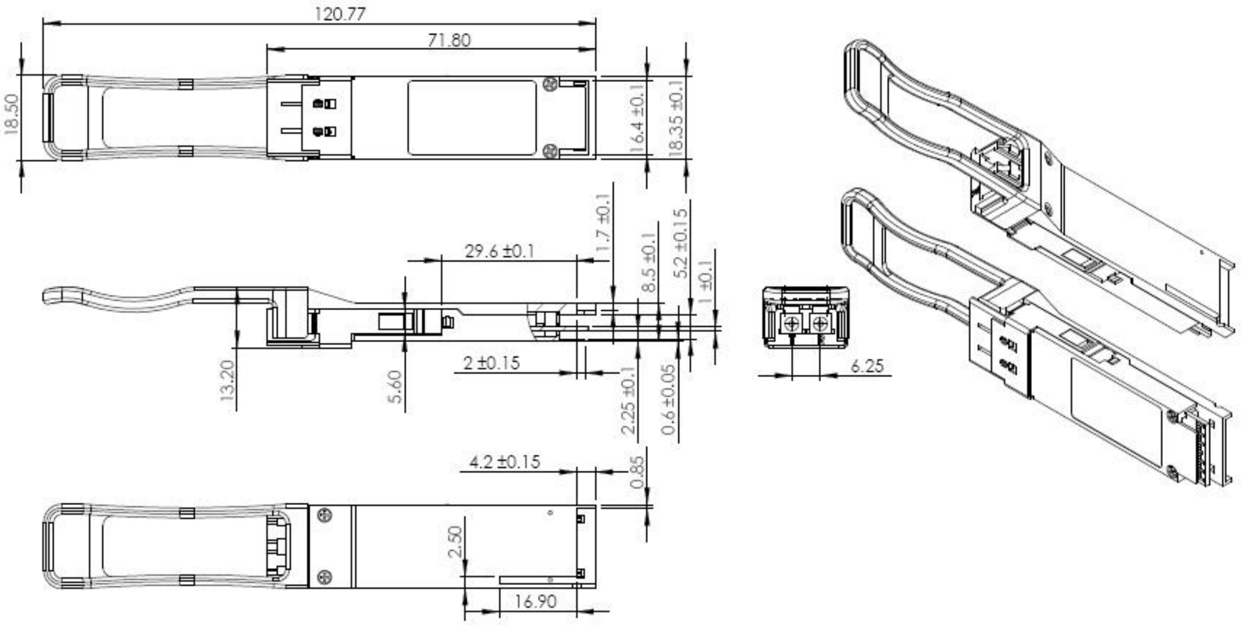
Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on[1], hot plug or rising edge of Reset until the module is fully functional[2]
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data ReadyTime	t_data	2000	ms	Time from power on[1] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional[2]
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode =Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	toff_IntL 500 μs Time from clear on read[3] operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted

Mask Assert Time	ton_mask	100	ms	Time from mask bit set[4] until associated IntL assertion is inhibited
Mask De-assert Time	toff_mask	100	ms	Time from mask bit cleared[4] until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	µs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	µs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set[4] until module power consumption enters lower Power Level
Power_over-ride or Power-set De-assert Time	toff_Pdown	300	ms	Time from P_Down bit cleared[4] until the module is fully functional[3]

Notes:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate per Lane	Laser	Optical Power	Detector	Receiver Sensitivity	Temp	Reach	Other	Application code
WST-QS28-SRB-C	**QSFP28**	**25.781 Gbps/ 10.312Gbps in optical**	**VCSEL**	**-6~ +4 dBm per Channel**	**PIN**	**-11 dBm per Channel**	**0~70°C**	**70m Via OM3, 100m via OM4**	**RoHS**	**100G/40G Ethernet**

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	21-Apr-2021	New Issue	Shao yu Lee	Wayne Liao	Wayne Liao
V1.1	10-May-2021	Update Product Characteristics	Shao-Yu Lee	Wayne Liao	Wayne Liao
V1.2	10-Sep-2021	Update Description	Shao-Yu Lee	Wayne Liao	Wayne Liao

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