WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

400G QSFP-DD SR8 Optical Transceiver Module
P/N: WST-QD4-SR8-C

Features:

- Hot Pluggable QSFP-DD form factor
- Supports 425Gb/s aggregate bit
- Low Power Dissipation, Max. 8W
- Single MPO16 receptacle
- Up to 70m transmission with OM3 multi-mode fiber and 100m transmission with OM4 multi-mode fiber.
- 8x50G PAM4 VCSEL/PIN photo detector
- Operating Case Temperature: 0~70℃
- Compliant to Class 1M Laser Safety
- ROHS: Environment Safety

Applications:

- Ethernet for 400GBASE-SR8
- HPC Interconnects
- Proprietary Interconnections

Standard:

- Compliant to QSFP-DD Rev 6.3
- CMIS Rev. 4.0 Management Interface
- SFF-8679: General Electrical
- IEEE 802.3bs: Physical Layer Specifications and Management Parameters

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Maximum Supply Voltage	V_{cc}	-0.5		3.6	V	
Storage Temperature	T_{sto}	-40		85	℃	
Case Operating Temperature	T_{op}	0		70	℃	
Relative Humidity	RH	0		85	%	1

Notes:

1. No-condensing.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Supply Voltage	V_{cc}	3.14		3.46	V	
Power Consumption	P_{Con}			8	W	
Bit Rate	BR		26.5625		GBd	1
Pre-FEC Bit Error Ratio	BER			$2.4x10^{-4}$		2
Post-FEC Bit Error Ratio				10^{-12}		
Center wavelength	λ_c	840		860	nm	3
Beam divergence angle			23		°	
Number of Lanes		8				
Transmit Distance	T_{D1}	0		70	m	OM3
	T_{D2}	0		100	m	OM4
Management Interface		Serial, I2C-based, maximum frequency 400 kHz				4
Logic Input Voltage High	V_{ih}	2		Vcc+0.3	V	
Logic Input Voltage Low	V_{il}	-0.3		0.8	V	

Notes:

1. Single lane
2. PRBS13Q test pattern is used.
3. As defined by IEEE Std. 802.3cd™ /D3.0
4. As defined by CMIS Rev. 4.0

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Transceiver Power Supply Current	I_{cc}			2400	mA	
Transmitter at TP1a						
AC common-mode output voltage (RMS)				17.5	mV	
Differential peak-to-peak output voltage (Transmitter disabled)				35	mV	
Differential peak-to-peak output voltage (Transmitter enabled)				880	mV	
Eye symmetry mask width	ESMW		0.22		UI	
Eye height, differential	EH	32			mV	

Differential output return loss		See Eq. 1				
Common to differential mode conversion return loss		See Eq. 2				
Differential termination mismatch				10	%	
Transition time (20% to 80%)	Tr, Tf	10			ps	
Receiver at TP4						
Far-end Eye height, differential		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential output return loss		See Eq. 1				
Common to differential mode conversion return loss		See Eq. 2				
Differential termination mismatch				10	%	
Transition time (20% to 80%)	Tr, Tf	10			ps	
DC common mode voltage		-350		2850	mV	

Notes:

1. $$RLd(f) \geq \begin{Bmatrix} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{Bmatrix} \text{ (dB)} \qquad \text{(Eq.1)}$$

   where

   f is the frequency in GHz, RLd is the CAUI-4 Chip-to-module input differential return loss

2. $$RLdc(f) \geq \begin{Bmatrix} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{Bmatrix} \text{ (dB)} \qquad \text{(Eq.2)}$$

   where *f* is the frequency in GHz, RLdc is the CAUI-4 Chip-to-module input differential to common mode input return loss

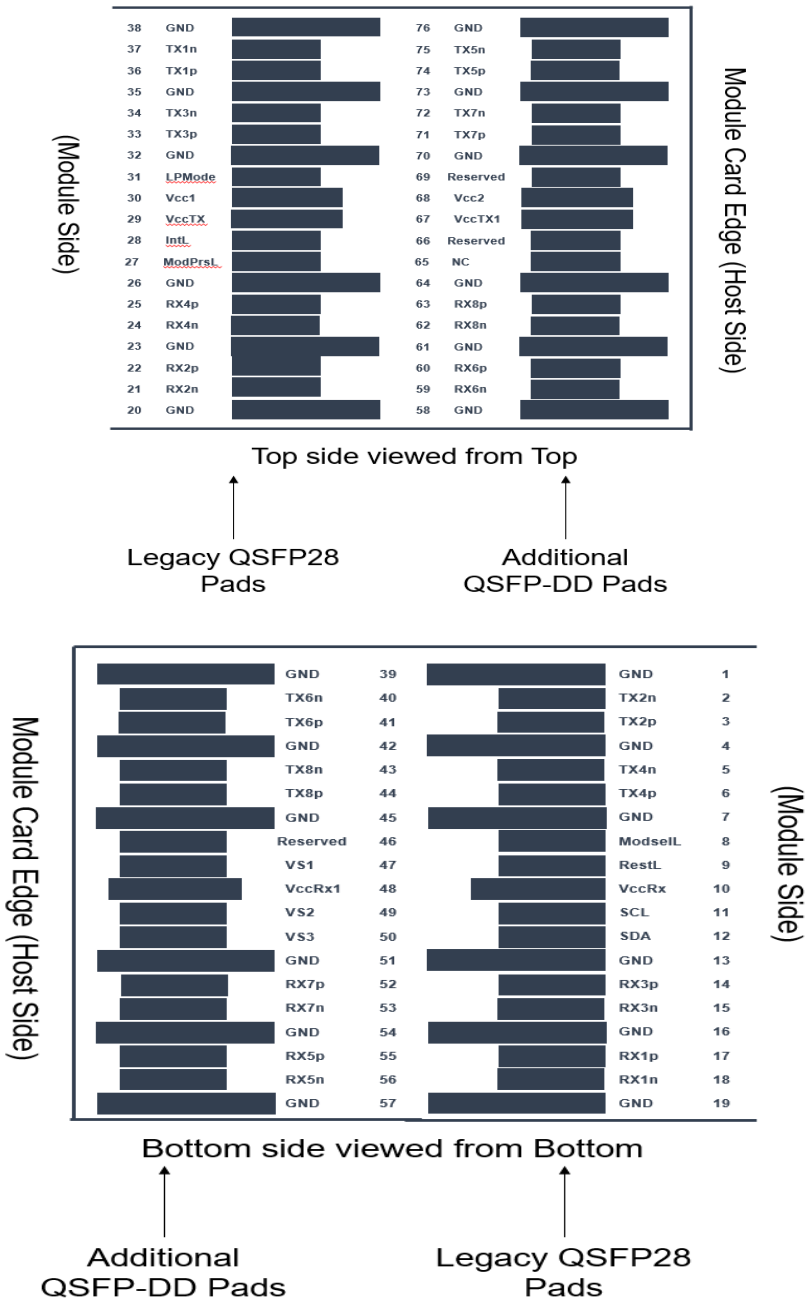
Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Transmitter						
Signaling Speed per Lane		26.5625 ± 100ppm			GBd	
Lane wavelengths (Range)	λ	840		860	nm	
RMS Spectral Width	△λ			0.6	nm	
Average launch power, each lane	P_{avg}	-6.5		4	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)		-4.5		3	dBm	
Transmit OMA per Lane	OMA	-6.4		3	dBm	
Transmitter and dispersion eye closure (TDEC), each lane	TDEC			4.5	dBm	
Launch power in OMA_{outer} minus TDECQ (min)		-5.9			dBm	
Extinction ratio	ER	3			dB	
Average launch power of OFF transmitter, each lane	P_{off}			-30	dBm	
Receiver						
Signaling Speed per Lane		26.5625 ± 100ppm			Gb/s	
Lane wavelengths (Range)	λ	840		860	nm	
Damage threshold		+5			dBm	
Average power at receiver input, each lane		-8.4		4	dBm	1
Receive Power, each lane (OMA)				3	dBm	
Receiver Reflectance				-12	dB	
Receiver sensitivity in OMA_{outer}				-3.4	dBm	2

Notes:

1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength.
2. Receiver sensitivity is informative and is defined for a transmitter with SECQ = 0.9 dB.

Pin Assignment



PIN	Symbol	Description	Ref.
1	GND	Ground	1
2	TX2n	Transmitter Inverted Data Input	

3	TX2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	TX4n	Transmitter Inverted Data Input	
6	TX4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc RX	+3.3V Power Supply Receiver	2
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	RX3p	Receiver Non-Inverted Data Output	
15	RX3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	RX1p	Receiver Non-Inverted Data Output	
18	RX1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	RX2n	Receiver Inverted Data Output	
22	RX2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	RX4n	Receiver Inverted Data Output	
25	RX4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc TX	+3.3V Power supply transmitter	2
30	Vcc1	+3.3V Power supply	2
31	LPMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	

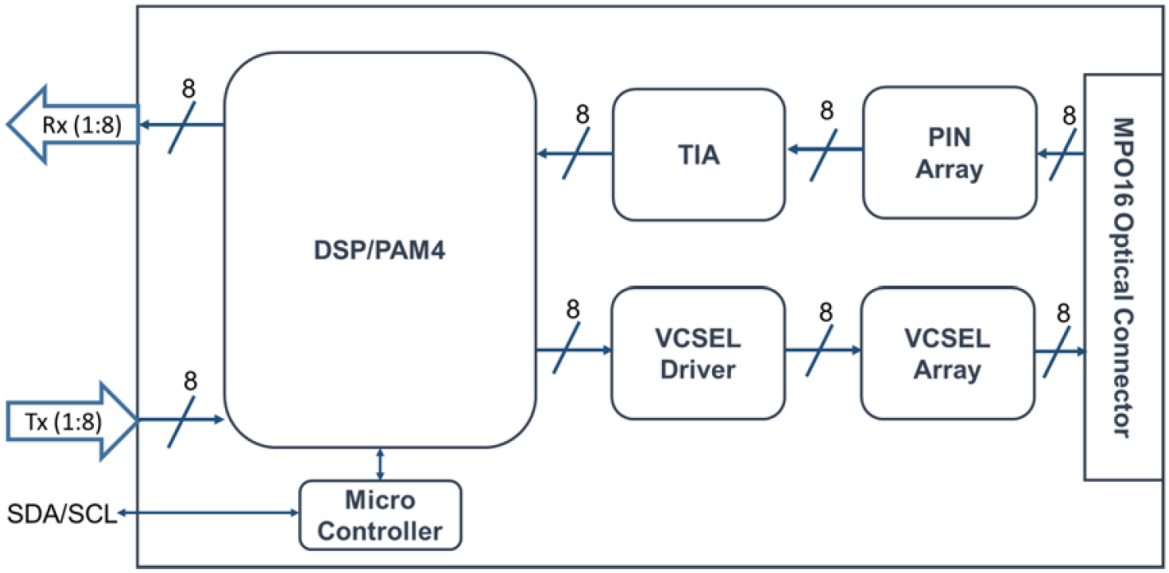
32	GND	Ground	1
33	TX3p	Transmitter Non-Inverted Data Input	
34	TX3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	TX1p	Transmitter Non-Inverted Data Input	
37	TX1n	Transmitter Inverted Data Input	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data Input	
45	GND	Ground	1
46	Reserved	For future use	3
47	VS1	Module Vendor Specific 1	3
48	3.3V Power Supply	2A	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1

62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For future use	3
67	VccTx1	3.3V Power Supply	2
68	Vcc2	3.3V Power Supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	1

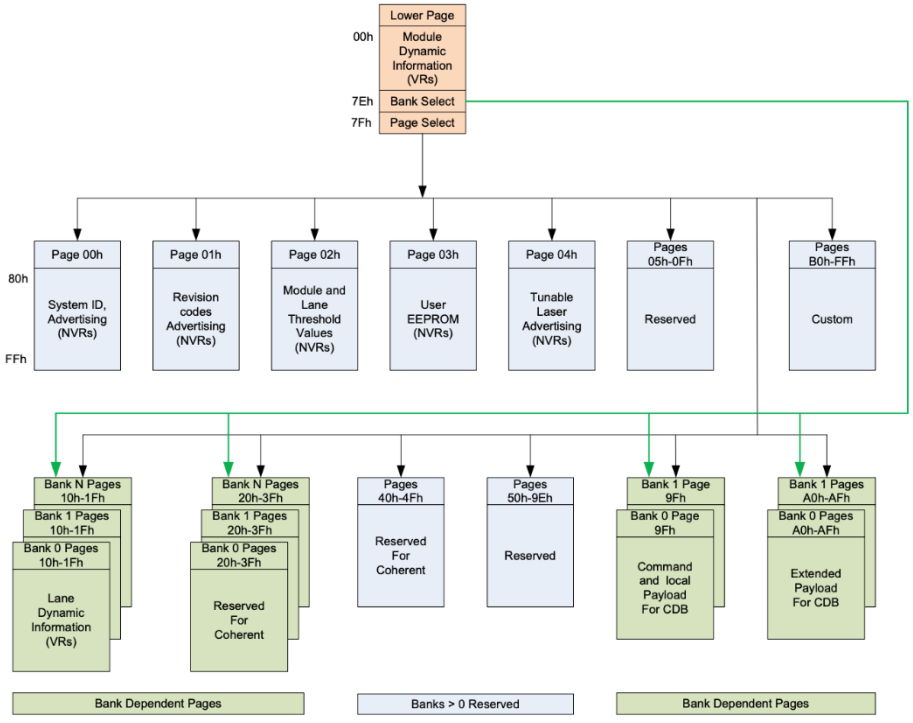
Notes:

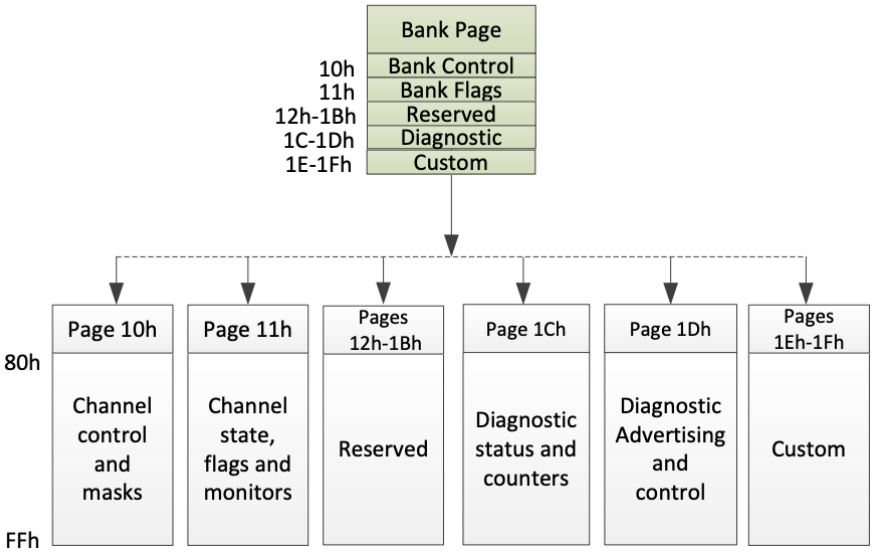
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc ping are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50ohms to grounds on the host. Pad 65 (No connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10k ohms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, the break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Recommended Host Block Diagram

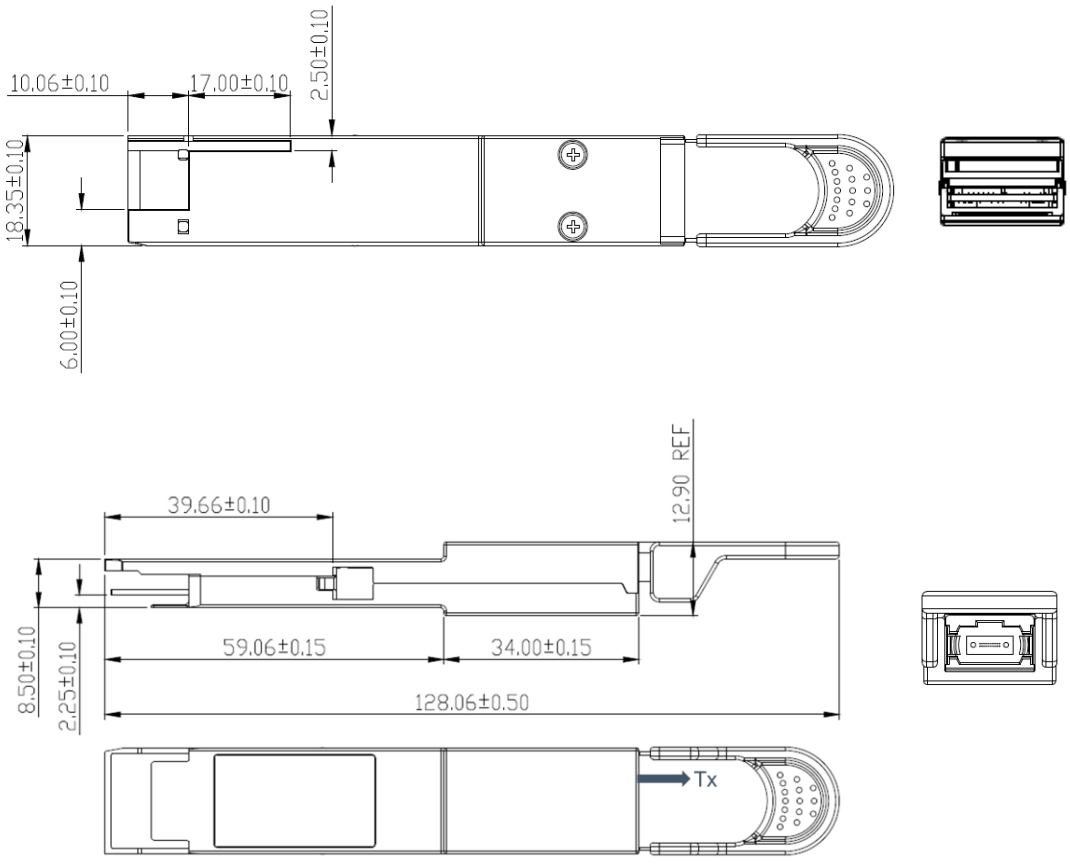


Memory map (compliant CMIS 4.0)





Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate	Laser	Optical Power	Detector	Max. Receive Sensitivity (OMA)	Temp	Reach	Other	Application code
WST-QD4-SR8-C	QSFP-DD	26.5625 Gbps each Channel	850nm VCSEL	-6.5~ +4 each Channel	PIN	-3.4 dBm each Channel	0~70°C	70m via OM3; 100m via OM4	DDM RoHS	400G Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	21-Jun-2019	New Issue	Ivy Chen	Wayne Liao	Wayne Liao
V1.1	03-Jun-2020	Update Memory Map	Ivy Chen	Wayne Liao	Wayne Liao
V1.2	09-Jul-2021	Update Power Consumption Typ.: 8W, Max.: 8.5W	Shao Yu Lee	Tom Tang	Wayne Liao
V1.3	17-Mar-2023	Update Format	Shao Yu Lee	Tom Tang	Wayne Liao
V1.4	13-Apr-2023	Update Power Consumption	Shao Yu Lee	Tom Tang	Wayne Liao

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